An FSK Telemetry Module for Vector Measuring Current Meters

by

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Technical Report

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Robert C. Beardsley, Chairman
Department of Physical Oceanography
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1.0 Abstract:

The EG&G Vector Measuring Current Meter (VMCM) used in mooring work provides a 20 ma Serial ASCII Instrumentation Loop (SAIL) communication system. A projected application of the VMCM is to have a surface mooring communicate with a series of VMCMs via a Frequency Shift Keying (FSK) link. While an FSK modem can communicate with the VMCM, a problem exists with the general operation of the VMCM. If the VMCM is addressed to dump data, it remains on until the unit is re-addressed. If a failure in the link occurs, then the VMCM stays on in a higher power mode and the batteries will be depleted early.

The insertion of a processing block between the modem and the VMCM provides a way to look at incoming data, qualify it and re-transmit it to the VMCM. The VMCM will reply and the preprocessor can channel the data to the modem. In the event of a VMCM malfunction, the preprocessor has a timeout function and will turn off the carrier keeping the line quiet.
2.0 Description of Technique:

An application of this instrument is to have a master controlling computer mounted on a surface float. Typically 4 or more VMCMs will be supported on a power bearing cable. Impressed on the power cable will be the FSK signal. At regular intervals the top unit will interrogate the lower units using the SAIL protocol.

When a carrier is not present on the line, the lower units remain in a sleep mode. When a carrier appears, the preprocessing units only will wake up for operation. With FSK communications data is impressed upon a carrier generated by the transmitting unit. The receivers must have their carrier off when listening. It is important that the carrier is generated for a short period prior to transmission so the receiving modems can phase lock on the signal.

The FSK protocol requires that the controller establish a carrier and then send the interrogation request. If the preprocessor recognizes the address as its own, it re-transmits it to the VMCM. All the other VMCMs on the line will remain quiet. The activated VMCM will be operating in the record buffer dump or "R" mode. Each time a new set of data becomes available, it is transferred to this buffer. When requested by "R" the buffer is normally sent via the SAIL 20 ma current loop. The preprocessor follows the logic level of this signal and transmits it via the modem to the surface.

After all activity in the VMCM has ended, the preprocessor has a software timeout function that sends an end of transmission character (ETX 03H), places the VMCM in its low power mode, and then shuts itself down. If the VMCM should hang up or develop an error during transmission, this timer will time out and shut the system down.
3.0 Description of Hardware:

The FSK SAIL Preprocessor card contains two sections, the FSK modem that provides logic level and FSK I/O and the microprocessor (uP) section that handles logical functions.

The FSK modem is based on the RELAYS Listening Station (RLS) modem. A single FSK line and 4 data I/O/control lines are provided in addition to a +5 volt supply and ground. The modem is shown in Figure 3.1.

With XMIT bar high the modem is in the receive mode. When a carrier is present, carrier detect goes high. Data out is a logic level high for a break condition. With XMIT bar low, the modem generates a carrier, carrier detect goes high, and data can be impressed on the carrier with a logic high being a break (low) condition.

The second part is the uP that controls the modem and communicates with the VMCM. It is based on the 146805E2 low power uP and in this configuration features 2K of ROM, a 2.4576 mHz clock, and reset on power up. It is shown in Figure 3.2.

The CPU will start operation 500 uSec after power has been established by the RC network driving CPU pin 1. The crystal frequency selected for the uP is based on the requirement to generate a 153.6 kHz timebase for the modem. A CD4040BE divides the uP Clock (uClock) by 16 down to the modem Clock (mClock). An 8 pole single throw DIP switch connected to Port A is used to set the SAIL address in the range of 00 to FF. The common side of the switches is driven by PB5 to reduce power consumption at the pull down resistors on Port A. When reading the SAIL address switches, PB5 is raised, Port A is read, and PB5 is lowered. Otherwise the worst case dissipation would be 133 uWatts. The switch positions are shown in Figure 3.3.

The modem control lines SDO, SDA, XMIT bar, and Carrier Detect are wired directly to the uP. The Carrier Detect is used to generate the interrupt to wake up the uP. The 146805E2 requires a low level to generate interrupts, so an XOR gate is set as an inverter to provide the correct logic level.

Communication with the VMCM is made by two serial I/O lines. The serial data from the VMCM is taken directly from the VMCM UART (SDO). By placing an open collector NPN transistor in parallel with the output NPN of the 20 ma current loop optoisolator, SAIL commands can be sent to the VMCM using logic levels. A software UART is used in the 146805E2. The VMCM SDI is driven by PB6. Operation of the 20 ma loop is allowed for diagnostic purposes when a carrier is not present. All signal connections to the preprocessor and the VMCM are shown in Figure 3.4. Backplane cut and jumper modifications are shown in Figure 3.5.
Suggested Penetration

Sea com dual sail penetrator

Dwg 0 6620-001


Place dip switch with T0Y position towards CPU

Component positions are shown for reference only.

High order address

Low order address

Low high

Sail address switch

Pressure housing penetrations and backplane connections

Top

Conductivity (opt)

Motor interface

ADC

Transport

Microprocessor

Serial interface

Sail FSK preprocessor

Compass interface

Compass analog

Card placement

Woods Hole Oceanographic Institution
Department of Physical Oceanography

Sail address switch setting, cable connection, and card placement

Contract 18/1984.46
Code no.

Paul D. Fucile
Date 10/25/87
Side B

Dwg no.

Switch

1 of 1

A
ALL COMPONENTS ARE REFERENCED TO
EG&G VMCM HARDWARE MANUAL
SERIAL CARD

TO PIN 14, U4

TO PIN 11, U3

VMCM SDI - TO CPU
NPN COLLECTOR AT
EDGE CONNECTOR 35

VMCM SDO - TO CPU PIN 29
(PB7) AT EDGE CONNECTOR 33

Figure 3.4 Preprocessor to VMCM Connections
------ JUMPER WIRE

X FOIL CUT

FIGURE 3.5 VMCM BACKPLANE MODIFICATION
The program is held in a 27C16 EPROM. The 146805E2 also provides 64 RAM locations for variables. Component placement is shown in Figures 3.6 and 3.7. The FSK board mounts in position J8 and placement is shown in Figure 3.3. Foil patterns are shown in Figures 3.8 and 3.9.
CAPACITOR, UNDERBOARD JUMPERS

CAPACITORS PLACED ON TOP

J2 (UNDERNEATH)

J1 (UNDERNEATH)

C11

C12

C13

C14

U1

U5

U6

U8

Q6

D7

Figure 3.7 Component Placement
4.0 Software:

The Software for the preprocessor is best described in terms of a flowchart and an assembly listing. Before describing the flowchart, some operational considerations should be mentioned. The 146805E2 supports low power STOP and WAIT commands. These commands allow the uClock to be stopped or removed from the uP architecture respectively. To simplify hardware, a software UART is being used for reception and transmission of 300 Baud data. The program must have features that prevent either the uP or VMCM from staying on in the event of a communications failure. The modem default must always be in the receive mode. Diagnostics should be available for other program development.

The flowchart is shown in Figure 4.1. On power up the two I/O ports data direction registers are set, Baud rate values are placed in RAM, the stack pointer is reset, and a "*" is sent via FSK out the modem indicating a good power up. After this the 146805E2 enters its lowest power mode by shutting off the carrier and the clock. On the detection of an FSK carrier a hardware interrupt occurs. The clock starts and the program vectors off to ROM location 1840H to start subroutine SALREC to qualify a valid SAIL address. If a different address is received or if a carrier drop is detected momentarily, then the 146805E2 returns to sleep.

Two timing registers are used to prevent the processor from staying on in the event of a modem or VMCM glitch. The subroutine MGET increments a counter while waiting for the first incoming character, otherwise the software UART would remain cycling continuously looking for the start bit. If a valid address occurs, then the carrier is turned on looking up to establish a good carrier in the line. The address is then regenerated along with the delimiter to the VMCM. The VMCM will reply with a string of data followed by a carriage return/line feed.

The transfer of data from the VMCM to the modem is performed by following the transitions at the SDO of the VMCM. The VMCM UART must see the data it transmits, so the transitions are sent to the VMCM SDI. The subroutine CIRCLE performs this function. While this routine is CIRCling, a counter register is being incremented. The maximum timeout is in the order of 600 mS. This is intended to prevent glitches in the VMCM data stream from hanging up the preprocessor. After the data transfer and clock timeout, the preprocessor is ready to enter a sleeping mode. An ETX (03H) is sent via FSK out the modem, the carrier is turned off looking up, and the NPN transistor in parallel with the SAIL 20 ma optoisolator is placed in a high impedance state. The STOP command is given and the preprocessor enters its low power mode.

The utilities used in this program are a subset of the ONSET 6805 monitor. These utilities are copyright protected and are used with the permission of Onset Computer Corporation. This includes the software UART, string handlers, and memory value handlers. The only utilities used in the FSK portion of the program are the UART GET and SEND routines. These routines have
also been modified and also appear as MGET and MSSEND.

A change in the hardware reset vector will cause the program to start in the monitor mode for diagnostics. The serial communications for the monitor are handled through the communications port PB7 and PB6. The monitor allows for memory location changes, data dumps, and execution of programs from RAM or ROM.

The assembly listing is given in Appendix A.
5.0 Installation and Tuning Procedures

The modem on the preprocessor requires tuning before installation. The equipment required includes:

A) Dual Power Supply
B) Frequency Counter
C) Storage Oscilloscope
D) FSK Deck Box
E) Decade Resistance Box
F) Terminal, 300 BAUD
G) Digital Voltmeter
H) Signal Generator, 1700 Hz.

Prior to powering up, a digital voltmeter set in the 200 mV range should be placed across the 2.7 Ohm sense resistor to monitor board current. The board should not exceed 3.7 mA (10 mV). Nominal current with the microprocessor installed and the board in the STOP mode is 2 mA (5.4 mV) and 10 mA (27 mV) when active.

Remove the 146805E2 microprocessor prior to tuning. Using a logic clip bring pin 8, IC7 high through a 10K 1/4W resistor to V+. This brings XMIT bar high.

5.1 Set Power Supply to +5.00 Volts and +2.90 Volts

5.2 Apply 5 Volts at V+ (pin 5) and GND (pin 1) of the Board.

5.3 Using a 16 Pin IC Clip on IC9 (4046), ground pin 9.

5.4 Install Decade Resistance Box in place of R54 (GND and Pin 12, IC9). Set at approximately 400K.

5.5 Place input to Frequency Counter at pin 3, IC9.

5.6 Adjust Decade Box for frequency count of 500 Hz +/- 10 Hz. Let this run for 5 minutes to verify stability.

5.7 Install 1% resistor with Decade Box value in R54 position. (Note 2).

5.8 Measure frequency.

5.9 Power down, disconnect GND from IC 9 pin 9.

5.10 Install Decade Resistance Box in place of R55 (GND and pin 11, IC9).

5.11 Power up, and apply +2.90 Volts to IC9, pin 9. Adjust Decade Resistance Box for a frequency of 1700 Hz +/- 10 Hz at pin 3, IC9.

5.12 Install 1% resistor with Decade Box value in R55 position. (Note 1).
5.13 Measure frequency.

5.14 Procedure for testing FSK serial data and tuning amplifiers follows.

5.15 Connect the signal generator to pins 33 (signal) and 35 (GND) of the modem board. Set the generator to 1700 Hz with an output voltage of 200 mV p-p.

5.16 Power up board.

5.17 Using the decade resistor box, select R37 for a symmetrical output at IC5, pin 10 (LM 346).

5.18 Install 1% resistor in R37 position. (Note 3).

5.19 Connect FSK Deck Box in place of the signal generator. Type a capital "U" on the terminal and verify a 5 Volt square wave is present at IC5, pin 10.

5.20 Set positive supply at 5.5 Volts.

5.21 With the storage oscilloscope, monitor IC5, pin 7. Send a "U" on the terminal and adjust R43 for a rising edge on the carrier detect. Continue to adjust R43 until carrier detect fails and set at midrange.

5.22 With the storage oscilloscope, monitor IC5, pin 1. Send a "U" on the terminal and adjust R44 for a square wave output on the data line. Continue to adjust R44 until data fails and set to midrange.

5.23 Refer to Figure 5.1 for the relationships between carrier and data.

5.24 Test modem operation over input voltage range of 4.9 to 6.3 Volts. Trim R44 (data) for optimum response over this range. Note: The limiting factor is the 4046 PLL which is not rated for operation below 5.0 Volts.

5.25 Insert the microprocessor on the Modem board and install in a modified VMCM using an extender card.

5.26 Turn on power. The Modem should send a "*" to the terminal via the FSK port.

5.27 Connect the DVM across the 2.7 Ohm sense resistor. Send the instrument address followed by the delimiter "R". The instrument should respond with its data buffer. The voltage across the 2.7 Ohm resistor is an indication of the board current. Verify that it returns to the prior quiescent value after sending the data and timing out (around 5 seconds). Note: The instrument address and "R" delimiter must be entered within a 2 second period or the program will time out.
Figure 5.1
Carrier Detect and Data Signals
## 6.0 Parts List and Component Placement

<table>
<thead>
<tr>
<th>Description</th>
<th>Quantity</th>
<th>Placement</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RESISTORS</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 Ohm 5% 1/4W</td>
<td>10</td>
<td>R10, R12 - R20</td>
</tr>
<tr>
<td>4.7K 5% 1/4W</td>
<td>1</td>
<td>R7</td>
</tr>
<tr>
<td>10K 5% 1/4W</td>
<td>3</td>
<td>R22, R23, R24 (option)</td>
</tr>
<tr>
<td>10M 5% 1/4W</td>
<td>2</td>
<td>R34, R6</td>
</tr>
<tr>
<td>1M 5% 1/4W</td>
<td>2</td>
<td>R26, R31</td>
</tr>
<tr>
<td>5.1K 1% 1/8W</td>
<td>2</td>
<td>R27, R28</td>
</tr>
<tr>
<td>3.3K 5% 1/4W</td>
<td>1</td>
<td>R29</td>
</tr>
<tr>
<td>51 Ohm 5% 1/4W</td>
<td>2</td>
<td>R35, R30</td>
</tr>
<tr>
<td>33K 5% 1/4W</td>
<td>1</td>
<td>R38</td>
</tr>
<tr>
<td>499K 1% 1/4W</td>
<td>3</td>
<td>R32, R33, R36</td>
</tr>
<tr>
<td>825K 1% 1/4W</td>
<td>1</td>
<td>R53</td>
</tr>
<tr>
<td>4.7M 5% 1/4W</td>
<td>1</td>
<td>R5</td>
</tr>
<tr>
<td>1.5M 5% 1/4W</td>
<td>2</td>
<td>R48, R50</td>
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<tr>
<td>562K 5% 1/4W</td>
<td>1</td>
<td>R49</td>
</tr>
<tr>
<td>7.5M 5% 1/4W</td>
<td>1</td>
<td>R45</td>
</tr>
<tr>
<td>200K 5% 1/4W</td>
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<td>R42</td>
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<td>470K 5% 1/4W</td>
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<td>R40</td>
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<tr>
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</tr>
<tr>
<td>562K 1% 1/8W</td>
<td>1</td>
<td>R52</td>
</tr>
<tr>
<td>820K 1% 1/8W</td>
<td>1</td>
<td>R39</td>
</tr>
<tr>
<td>1M 1% 1/8W</td>
<td>1</td>
<td>R47</td>
</tr>
<tr>
<td>100K 1% 1/8W</td>
<td>1</td>
<td>R46</td>
</tr>
<tr>
<td>SELECT 1% 1/8W</td>
<td>3</td>
<td>R37, R54, R55</td>
</tr>
<tr>
<td>2.7 Ohm 5% 1/4W</td>
<td>1</td>
<td>Rsense</td>
</tr>
<tr>
<td>10 PIN RES SIP 9-1M NETWORK</td>
<td>2</td>
<td>SIP1, SIP2</td>
</tr>
<tr>
<td>TEN TURN TRIMPOT 200K</td>
<td>2</td>
<td>R43, R44</td>
</tr>
</tbody>
</table>

| **SEMI-GONDUCTORS**                      |          |                  |
| 2.4576 MHz (CRYSTEK)                     | 1        | XTAL             |
| 1N914 DIODE                              | 3        | D8, D9, D7       |
| 2N3094 TRANSISTOR                        | 1        | Q8               |
| 2N2907 TRANSISTOR                        | 1        | Q6               |
| 2N2222 TRANSISTOR                        | 1        | Q7               |

<p>| <strong>CAPACITORS</strong>                           |          |                  |
| 22pF CM05ED 220J03 MICA                   | 2        | C1, C2           |
| 50uF @6v CDENLW50-6                       | 1        | C3, ELECTROLYTIC |
| 0.001uF POLYCARB 10%                     | 1        | C19              |
| 0.0012uF POLYCARB 10%                    | 1        | C18              |</p>
<table>
<thead>
<tr>
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<th>Quantity</th>
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<tbody>
<tr>
<td>0.0022uF POLYCARB 10%</td>
<td>1</td>
<td>C21</td>
</tr>
<tr>
<td>0.022uF WHITE POLYCARB 10%</td>
<td>1</td>
<td>C17</td>
</tr>
<tr>
<td>4.7uF CERAMIC</td>
<td>4</td>
<td>C13,C14,C11,C12</td>
</tr>
<tr>
<td>1.0uF CK05 CERAMIC</td>
<td>1</td>
<td>C20</td>
</tr>
<tr>
<td>0.01uF CK05 CERAMIC</td>
<td>1</td>
<td>C15</td>
</tr>
<tr>
<td>0.022uF CK05 CERAMIC</td>
<td>1</td>
<td>C16</td>
</tr>
<tr>
<td>0.1uF CK05 CERAMIC</td>
<td>1</td>
<td>C4</td>
</tr>
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**INTEGRATED CIRCUITS**

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<tr>
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<th>Quantity</th>
<th>Location</th>
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</thead>
<tbody>
<tr>
<td>CD4011BFX</td>
<td>1</td>
<td>U1</td>
</tr>
<tr>
<td>CD4013BE</td>
<td>2</td>
<td>U2,U6</td>
</tr>
<tr>
<td>CD40103BE</td>
<td>1</td>
<td>U3</td>
</tr>
<tr>
<td>CD4040BE</td>
<td>1</td>
<td>U4</td>
</tr>
<tr>
<td>LM346J</td>
<td>1</td>
<td>U5</td>
</tr>
<tr>
<td>CD4070BE</td>
<td>1</td>
<td>U7</td>
</tr>
<tr>
<td>MC146805E2</td>
<td>1</td>
<td>U8</td>
</tr>
<tr>
<td>CD4046BF</td>
<td>1</td>
<td>U9</td>
</tr>
<tr>
<td>27C16</td>
<td>1</td>
<td>U11</td>
</tr>
<tr>
<td>CD74HC573E</td>
<td>1</td>
<td>U12</td>
</tr>
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**JUMPERS**

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<tr>
<th>Description</th>
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<th>Location</th>
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<tbody>
<tr>
<td>PIN 5, U8 to PIN 9, U1</td>
<td>1</td>
<td>J1</td>
</tr>
<tr>
<td>PIN 4, U8 to PIN 8, U1</td>
<td>1</td>
<td>J2</td>
</tr>
<tr>
<td>PIN 1, U7 to PIN 12, U1</td>
<td>1</td>
<td>J3</td>
</tr>
<tr>
<td>PIN 3, U7 to PIN 2, U8</td>
<td>1</td>
<td>J4</td>
</tr>
<tr>
<td>R42-R41 NODE to R15-C17 NODE</td>
<td>1</td>
<td>J5</td>
</tr>
<tr>
<td>16 PIN DIPSWITCH</td>
<td>1</td>
<td>SW1 (U10)</td>
</tr>
</tbody>
</table>

EG&G Serial Card Jumpers:
All IC numbers refer to EG&G VMCM Hardware Manual designations.
Use #30 Gauge Kynar or similar wire.

J35 to Pin 10, U7 R11 node
J37 to Pin 13, U4 and Pin 6, U12

Make connections to resistors.
7.0 Recommendations

During the development of this board, two software changes have been discussed. The first is to replace the simple "*" instrument on greeting with a longer stream indicating SAIL switch setting, software version, and an instrument title. The second is to place parity with the data. This would involve storing the data as it comes in from the VMCM and regenerating this stream with the addition of parity bits. The problem with this method is there is a limit on memory space, and two bytes would have to be stored in one memory location. Presently the clear reception of the ETX at the end of the stream qualifies the data.

A use for the remaining port pin PB4, would be to determine if the program is going to be operational or diagnostic on power up. With this pin low (normal condition) the program would vector to the FSK program. If the pin was tied high and the system was reset, it would enter the diagnostic mode. This would include strings that can be sent out the FSK port, and other modem tuning related operations.

A hardware reduction scheme would be to have the software generate the FSK data. This would require the data to be stored prior to transmission. Then the microprocessor could generate the FSK frequencies.
8.0 References


8.2 Onset Computer Corporation, 199 Main Street, North Falmouth, Mass. 02556. (617) 563-2267.

; FILE - "VMCM5.ASM"
; PROGRAM FOR WHOI SAIL VMCM INTERFACE
; LAST ENTRY ON AUGUST 13, 1987
; ADDITIONAL CLEANUP ON NOV 23, 1987
; PAUL D. FUCILE, PHYSICAL OCEANOGRAPHY, WHOI
; THIS VERSION QUALIFIES THE "R" DELIMITER AND
; TRANSMITS AN ETX AT THE END OF A TRANSMISSION
; THIS PROGRAM USES A SOFTWARE TIMEOUT, UART,
; AND IMPLICIT OPERATIONS
; MARCH 17, 1986 - ONSET MONITOR ROUTINES
; APPENDED FOR VMCM WORK WITH PERMISSION
; MONITOR COPYRIGHT - ONSET COMPUTER CORPORATION

; ESTABLISH FIRST PAGE VARIABLES

0000   ADATA    EQU     00H
0001   BDATA    EQU     01H
000D   CR       EQU     0DH
000A   LF       EQU     0AH
0008   TDATA    EQU     8 ; TIMER DATA PORT
0009   TCNTRL   EQU     9 ; TIMER CONTROL PORT
0010   TIMA     EQU     10H ; TEMP STORAGE FOR TIMER COUNT
0011   TIMB     EQU     TIMA+1
0012   TTIMA    EQU     TIMB+1
0013   TTIMB    EQU     TTIMA+1
0014   TEMP1    EQU     TTIMB+1 ; TEMPORARY DATA STORAGE
0015   TEMP2    EQU     TEMP1+1
0016   TEMP3    EQU     TEMP2+1
0017   TEMP4    EQU     TEMP3+1 ; 10H THROUGH 22H USED
0018   TEMP5    EQU     TEMP4+1
0019   PROG1    EQU     TEMP5+1 ; 10 BYTE STORAGE FOR CODE
001D   PROG2    EQU     PROG1+4 ; 4 BYTE PROGRAM STORAGE
0021   PROG3    EQU     PROG2+4
0023   PROG4    EQU     PROG3+2 ; PROG4 USES 2 BYTES

002A   SAILHI   EQU     2AH
002B   SAILLO   EQU     2BH
002C   VCNTHI   EQU     2CH
002D   VCNTL0   EQU     2DH
002E   DLMTR    EQU     2EH ; DELIMITER AFTER VALID ADDRESS
002F   CNTRHI   EQU     2FH
0030   TYM1     EQU     30H
0031   TYM2     EQU     31H
0032   TYMTST   EQU     32H
0033   TRYTST   EQU     33H
0034   TWYTST   EQU     34H

DISABLE OPSYN SEI ; DISABLE INTERRUPTS
ENABLE OPSYN CLI ; ENABLE INTERRUPTS
SLEEP OPSYN STOP ; TURN PROCESSOR OFF
1800  ORG  1800H  ;START OF VMCM PROGRAM
1800  CD18E3  JSR  CONFIG  ;CONFIGURE I/O
1803  CD18DA  JSR  BDSET  ;SET BAUD RATE TO 300
1806  CD18F0  JSR  READ  ;READ SAIL ADDRESS SWITCHES
1809  9C  RSP  ;RESET STACK POINTER
180A  A62A  LDA  #'*'  ;SAYS HELLO TO SURFACE
180C  CD196F  JSR  MSEND
180F  9A  ENABLE
1810  8E  SLEEP
1840  ORG  1840H  ;HARDWARE INT ROUTINE
1840  9C  RSP
1841  1401  BSET  2,1  ;MAKE SURE MODEM IS LISTENING
1843  3F30  CLR  TYM1
1845  3F31  CLR  TYM2
1847  CD1926  SALREC:  JSR  MGET  ;LOOK FOR VALID SAIL ADDRESS
184A  A123  CMP  #'#'  ;LOOK FOR SAILHI
184C  26F9  BNE  SALREC
184E  CD1926  SAL2:  JSR  MGET  ;LOOK FOR SAILHI
1851  B12A  CMP  SAILHI
1853  2707  BEQ  SAL3
1855  A123  CMP  #'#'  ;LOOK FOR SAILLO
1857  26E9  BNE  SALREC
1859  CC184E  JMP  SAL2
185C  CD1926  SAL3:  JSR  MGET  ;LOOK FOR SAILLO
185F  B12B  CMP  SAILLO
1861  2707  BEQ  SAL4
1863  A123  CMP  #'#'  ;GET VMCM DELIMITER (R,D,...)
1865  26E9  BNE  SALREC
1867  CC184E  JMP  SAL2
186A  CD1926  SAL4:  JSR  MGET  ;STORE IT AWAY
186D  B72E  STA  DLTR  ;QUALIFY 'R' IMPLICITLY
186F  A152  CMP  #'R'  ;VALIDATE REGISTRATION
1871  2707  BEQ  SAL5
1873  A123  CMP  #'#'  ;VALIDATE REGISTRATION
1875  26D0  BNE  SALREC
1877  CC184E  JMP  SAL2
187A  CD190B  SAL5:  JSR  VMCMON  ;TURN VMCM ON
187D  1501  BCLR  2,1  ;TURN CARRIER ON LOOKING UP
187F  3F32  CLR  TYMTST  ;TWO TRY REGISTER
1881  3F34  CLR  TWYTST
1883  3F33  CLR  TRYTST
1885  CD1911  SSON:  JSR  SAILON  ;SEND GOOD SAIL ADDRESS THROUGH
1888  1C01  BSET  6,1  ;SEND DATA TO SURFACE
188A  3F30  CLR  TYM1

25
188C 3F31

188E 3C30  CIRCLE:  INC  TYM1
1890 B630  LDA  TYM1
1892 A1FF  CMP  #0FFH
1894 2608  BNE  Q3
1896 3C31  INC  TYM2
1898 B631  LDA  TYM2
189A A140  CMP  #40H
189C 271F  BEQ  QUIT

189E 0F01ED  Q3:  BRCLR  7,1,CIRCLE
18A1 1D01  BCLR  6,1
18A3 1301  BCLR  1,1
18A5 0E01FD  CIR2:  BRSET  7,1,CIR2
18A8 1C01  BSET  6,1
18AA 1201  BSET  1,1
18AC 3F30  CLR  TYM1
18AE 3F31  CLR  TYM2

18B0 3C32  INC  TYMTST
18B2 A63C  LDA  #60  ;60 DECIMAL TRANSITIONS QUALIFY
18B4 B132  CMP  TYMTST  ;AS A RESPONSE
18B6 2602  BNE  WIT7
18B8 3C33  INC  TRYST
18BA CC188E  WIT7:  JMP  CIRCLE  ;WAIT FOR NEXT RS-232 TRANSITION

18BD 3C34  QUIT:  INC  TWSTT
18BF B634  LDA  TWSTT
18C1 A104  CMP  #04H  ;CHANGED FROM TWO TO FOUR
18C3 2709  BEQ  QUIT5

18C5 A600  LDA  #00H  ;60 DECIMAL TRANSITIONS QUALIFY
18C7 B133  CMP  TRYST  ;AS A RESPONSE
18C9 26F2  BNE  QUIT
18CB CC1885  JMP  SON

18CE A603  QUIT5:  LDA  #03H  ;SEND ETX BEFORE SHUTTING DOWN
18D0 CD196F  JSR  MSEND  ;JUNE 10 ADDITION

18D3 1401  QUIT6:  BSET  2,1
18D5 2EF0  BIL  QUIT6  ;JUNE 19 ADDITION
18D7 1D01  BCLR  6,1  ;ALLOW 20 mA SAIL AFTER TIMEOUT
18D9 8E  SLEEP

;VMCM SUBROUTINES ARE CONTAINED HERE

18DA A600  BDSET:  LDA  #00H  ;SET BAUD RATE FOR 300
18DC B710  STA  TIMA  ;AT 2.4576 MHZ
18DE A6CC  LDA  #0CCH
18E0 B711  STA  TIMB
18E2 81  RTS

26
CONFIG: ;SET UP PORTS
;LISTING PORT PIN FUNCTIONS
;PORT A LINES ARE SAIL ADDRESSES HIGH TO LOW IN ORDER
;PB0 - FSK SAIL MODEM SDI (TIED TO IRQ) (IN)
;PB1 - FSK SAIL MODEM SDO (OUT)
;PB2 - XMIT BAR TO MODEM (OUT)
;PB3 - FSK CARRIER DETECT (IN)
;PB4 - NO CONNECTION - PAD PROVIDED (IN)
;PB5 - SAIL ADDRESS SWITCH POWER (OUT)
;PB6 - TO CURRENT LOOP SAIL CONTROL AND SDI (OUT) (VMCM)
;PB7 - FROM CURRENT LOOP SAIL SDO (IN) (VMCM)

18E3 A666 LDA #66H
18E5 B705 STA 5 ;SET OUTPUT LINES HIGH TO START
18E7 A606 LDA #06H
18E9 B701 STA 1 ;EXCEPT OPTO NPN SWITCH
18EB A600 LDA #00H
18ED B704 STA 4 ;PORT A ALL IN
18EF 81 RTS

18F0 1A01 READ: BSET 5,1 ;READ SAIL ADDRESS SWITCHES
18F2 9D NOP
18F3 9D NOP
18F4 B600 LDA ADATA
18F6 B72B STA SAILLO
18F8 1B01 BCLR 5,1
18FA 44 LSRA
18FB 44 LSRA
18FC 44 LSRA
18FD 44 LSRA
18FE AB30 ADD #30H ;MAKE ASCII EQUIVALENT
1900 B72A STA SAILHI
1902 A60F LDA #0FH ;MASK LOW SAIL ADDRESS
1904 B42B AND SAILLO
1906 AB30 ADD #30H ;MAKE ASCII EQUIVALENT
1908 B72B STA SAILLO
190A 81 RTS
190B A623 VMCMON: LDA "##" ;THIS WAKES THE VMCM UP
190D CD1F29 JSR SEND
1910 81 RTS
1911 A623 SAILON: LDA "##" ;RE-TRANSMIT ACCESS CODE TO VMCM
1913 CD1F29 JSR SEND
1916 B62A LDA SAILHI
1918 CD1F29 JSR SEND
191B B62B LDA SAILLO
191D CD1F29 JSR SEND
1920 B62E LDA DLMTR
1922 CD1F29 JSR SEND
1925 81 RTS
1926 3F30 MGET: CLR TYM1 ;FSK MODEM UART RECEIVE ROUTINE
1928 3F31 CLR TYM2 ;RAISE XMIT BAR

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192A 3C30 MGET1: INC TYM1 ;WAIT FOR START BIT AND TIMEOUT
192C B630 LDA TYM1
192E A1FF CMP #OFFH
1930 2608 BNE MGETX
1932 3C31 INC TYM2
1934 B631 LDA TYM2
1936 A1FF CMP #OFFH
1938 272E BEQ QUIT2 ;IF TIMEOUT GOTO SLEEP
193A 0001ED MGETX: BRSET 0,1,MGET1 ;WAITING FOR START BIT
193D BE10 LDX TIMA
193F B611 LDA TIMB ;WAIT 1/2 BIT CELL
1941 57 ASRX
1942 46 RORA ;DIVIDE BY 2
1943 A005 SUB #5 ;TIMING COMPENSATION
1945 2501 BCS MGET01
1947 5C INCX
1948 4C MGET01: INCA
1949 4A MGET02: DECA
194A 9D NOP
194B 26FC BNE MGET02
194D 5A DECX
194E 26F9 BNE MGET02
1950 AE80 LDX #80H ;BIT IN D7 IS FLAG
1952 CD1F55 MGET3: JSR TIMIN3 ;1 BIT CELL WAIT
1955 54 LSRX ;MOVE OVER FOR NEXT BIT
1956 250B BCS MGET4
1958 9D NOP
1959 9F TXA
195A 010102 BRCLR 0,1,MGET2 ;ADD NOTHING IF CLEAR
195D AB80 ADD #80H ;PUT IN BIT IF NOT
195F 97 MGET2: TAX
1960 9D NOP
1961 20EF BRA MGET3 ;QUIT WHEN ALL 7 DONE
1963 CD1F4D MGET4: JSR TIMIN1 ;WAIT ONE MORE CELL
1966 9F TXA
1967 81 MGET6: RTS
1968 1401 QUIT2: BSET 2,1 ;IF TIMOUT OCCURS, THEN
196A 2EFC BIL QUIT2
196C 1D01 BCLR 6,1 ;GOTO SLEEP
196E 8E SLEEP ;5 BIT DELAY
196F MSEND: ;FSK MODEM UART TRANSMIT ROUTINE
196F B715 STA TEMP2 ;SAVE CHARACTER
1971 1501 BCLR 2,1 ;LOWER XMIT BAR
1973 CD1F4D JSR TIMIN1
1976 CD1F4D JSR TIMIN1

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1979 CD1F4D          JSR  TIMIN1
197C CD1F4D           JSR  TIMIN1
197F CD1F4D           JSR  TIMIN1
1982 B615             LDA  TEMP2
                      
1984 1301             BCLR  1,1
1986 AA80             ORA  #80H
1988 97               TAX
1989 CD1F55           JSR  TIMIN3
                      ;WAIT FOR TIMEOUT
198C 54               LSRX
198D 270A             BEQ  MSEND3
198F 2404             BCC  MSEND2
1991 1201             BSET  1,1
1993 20F4             BRA  MSEND1
                      ;SET TRANSMITTED BIT
1995 1301             MSEND2:  BCLR  1,1
1997 20F0             BRA  MSEND1
                      ;CLEAR TRANSMITTED BIT
1999 1301             MSEND3:  BCLR  1,1
199B CD1F51           JSR  TIMIN2
199E 1201             BSET  1,1
19A0 CD1F4D           JSR  TIMIN1
19A3 B615             LDA  TEMP2
19A5 1401             BSET  2,1
19A7 81               RTS
                      ;FOR STOP BIT
                      ;WAIT FOR STOP BIT END
                      ;RECOVER CHARACTER
                      ;RAISE XMIT BAR
                      ;MODIFIED GET ROUTINE
19A8 0E01FD           VGET:  BRSET  7,1,VGET
19AB B610             LDX  TIMA
19AD B611             LDA  TIMB
19AF 57               ASRX
19B0 46               RORA
19B1 A005             SUB  #5
19B3 2501             BCS  VGX1
19B5 5C               INCX
19B6 4C               VGX1:  INCA
19B7 4A               VGX2:  DECA
19B8 9D               NOP
19B9 26FC             BNE  VGX2
19BB 5A               DECX
19BC 26F9             BNE  VGX2
19BE AE80             LDX  #80H
19C0 CD1F55           VG3:  JSR  TIMIN3
19C3 54               LSRX
19C4 250B             BCS  VG4
19C6 9D               NOP
19C7 9F               TXA
19C8 0F0102           BRCLR  7,1,VG2
19CB 880              ADD  #80H
19CD 97               VG2:  TAX
19CE 9D               NOP
19CF 20EF             BRA  VG3
19D1 CD1F4D           VG4:  JSR  TIMIN1
19D4 9F               TXA
19D5 81               VG6:  RTS
                      ;MODIFIED FOR LOWER CASE CHARS
19D6 0E01FD EGET:   BRSET 7,1,EGET ;MODIFIED GET ROUTINE ECHOES
19D9 BE10 LDX TIMA ;CHARACTERS IMMEDIATELY
19DB B611 LDA TIMB
19DD 57 ASRX
19DE 46 RORA
19DF 46 RORA
19E0 46 RORA
19E1 A005 SUB #5
19E3 2501 BCS EGX1
19E5 5C INCX
19E6 4C EGX1: INCA
19E7 4A EGX2: DECA
19E8 9D NOP
19E9 26FC BNE EGX2
19EB 5A DECK
19EC 26F9 BNE EGX2 ;ADDED STATEMENT
19EE 1D01 BCLR 6,1
19F0 AE80 LDX #80H
19F2 CD1F55 EG3: JSR TIMIN3
19F5 54 LSRX
19F6 2512 BCS EG4
19F8 9D NOP
19F9 9F TXA
19FA 0F0107 BRCLR 7,1,EG2 ;ADDED STATEMENTS
19FD AB80 ADD #80H
19FF 1D01 BCLR 6,1
1A01 CC1A06 JMP EG9
1A04 1C01 EG2: BSET 6,1
1A06 97 EG9: TAX
1A07 9D NOP
1A08 20E8 BRA EG3
1A0A 1C01 EG4: BSET 6,1
1A0C CD1F4D JSR TIMIN1
1A0F 1D01 BCLR 6,1 ;ATTEMPT TO ADD STOP BIT
1A11 9F TXA ;MODIFIED FOR LOWER CASE CHARS
1A12 81 EG6: RTS

1D00 ORG 1D00H ;START OF MONITOR ROM

;MONITOR OPERATIONS
;THIS MONITOR DETERMINES BAUD RATE BY TIMING A
;CARRIAGE RETURN ON A RESET. THE OPERATORS ARE:
;D - DISPLAY 16 MEMORY LOCATIONS FROM STARTING
;ADDRESS FROM XXXX
;S - SUBSTITUTE MEMORY LOCATION (A %CR% DOES
;NOT ALTER MEMORY)
;G - GO, EXECUTE A PROGRAM RESIDING AT XXXX
;TO EXIT AN OPERATOR, ENTER A DECIMAL POINT "." OR RESET

;SET UP PORTS - ALWAYS COPY SUBROUTINE 'CONFIG' SETUP

1D00 A666 START: LDA #66H ;SET DATA DIRECTION OF PORT B
STA 5 ;TO 01100110 1 = OUTPUT
LDA #46H ;SET OUTPUT LINES HIGH TO START
STA 1 ;AND XMIT BAR ALSO
LDA #00H ;SET DDR OF PORT A TO ALL IN
STA 4

JSR BDSET ;FOR 300 BAUD - COMMENTED OUT
JSR RATSET ;AUTO BAUD SETTING ROUTINE

LDA #HIGH SIGNON
LDA #LOW SIGNON

JSR SNDSTG
JMP MONITR

SIGNON: DB '*VMCM SAIL PREPROCESSOR*$'

MONITR: RSP ;RESET STACK
JSR CRLF ;EACH NEW COMMAND STARTS WITH
LDA #'!'; (RET), '!' ;
JSR SEND

GET ;GO THROUGH LIST

SIGN10: JSR

DOTD: CMP #'D'
BNE DOTG
JMP DISP

CMP #'G'
BNE DOTS
JMP GOTO

CMP #'S'
BNE SIGN10
JMP SUBST

DISP: JSR PREP ;ECHO COMMAND, GET ADDRESS
DISP0: JSR SNDAD ;SHOW ADDRESS FIRST
JSR SND2SP
LDA #16 ;SET UP LOOP COUNTER
STA TEMP4 ;USE TEMP4
JSR SAVAD

DISP1: JSR GETM
JSR SNDBY
JSR SNDSP
JSR INCAD
DEC TEMP4 ;LOOP TILL BYTES SHOWN
BNE DISP1
JSR SND2SP ;ADD 2 SPACES
JSR RECAD ;RECOVER ADDRESS FROM PROG4
LDA #16
STA TEMP4 ;RESET COUNTER
JSR GETM ;GET BYTE AGAIN
CMP #20H ;SHOW THEM AS ASCII CHARACTERS
BCC DISP2 ;UNLESS CONTROL
LDA #'.' ;-SHOW THOSE AS '.'
CMP #7FH
BCS DISP4
1D8A  A62E     LDA      #','
1D8C  CD1F29   JSR      SEND
1D8F  CD1E35   JSR      INCAD
1D92  3A17     DEC      TEMP4    ;DO TILL DONE
1D94  26E7     BNE      DISP3
1D96  CD1DF5   JSR      CRLF
1D99  CD1EFB   JSR      GET      ;ESCAPE ON INCOMING '.'
1D9C  A12E     CMP      #','
1D9E  26B6     BNE      DISPO
1DA0  CC1D32   JMP      MONITR

1DA3  CD1DE0   GOTO:    JSR      PREP      ;ECHO COMMAND, GET ADDRESS
1DA6  CD1E6A   JSR      SNDAD      ;SHOW ADDRESS FIRST
1DA9  CD1DF5   JSR      CRLF      ;GO AFTER CR
1DAC  CD1E45   JSR      GOMEM

1DAF  CD1DE0   SUBST:   JSR      PREP      ;ECHO COMMAND, GET ADDRESS
1DB2  CD1E6A   SUBST1:  JSR      SNDAD      ;SHOW ADDRESS FIRST
1DB5  CD1DEA   JSR      SND2SP     ;THEN 2 SPACES
1DB8  CD1E4D   JSR      GETM      ;GET BYTE
1DBB  CD1E58   JSR      SAVAD      ;SAVE PROG1 ADDR IN PROG4 ADDR
1DBE  B71B     STA      PROG1+2   ;FOR DEFAULT START OF GETAD1
1DC0  CD1E75   JSR      SNDBY      ;SHOW IT
1DC3  CD1DEA   JSR      SND2SP     ;ADD 2 SPACES
1DC6  CD1E96   JSR      GETAD1     ;GET NEW VALUE
1DC9  B61B     LDA      PROG1+2   ;GET DATA
1DCA  CD1E61   JSR      RECAD      ;BRING BACK ADDRESS
1DCE  CD1E49   JSR      PUTM      ;INSTALL NEW BYTE
1DD1  CD1DF5   JSR      CRLF
1DD4  CD1E35   JSR      INCAD
1DD7  20D9     BRA      SUBST1

;*************MISC GENERAL SUBROUTINES***************

1DD9  CD1F29   ECHO:    JSR      SEND      ;ECHO INCOMING CHARACTER
1DDC  CD1DF5   JSR      CRLF
1DDF  81       RTS

1DE0  CD1DD9   PREP:     JSR      ECHO
1DE3  CD1E92   JSR      GETAD      ;GET ADDRESS TO PROG1+1
1DE6  CD1DF5   JSR      CRLF      ;& PROG+2
1DE9  81       RTS

1DEA  A620     SND2SP:   LDA      #','
1DEC  CD1F29   JSR      SEND
1DEF  A620     SNDSP:    LDA      #','
1DF1  CD1F29   JSR      SEND
1DF4  81       RTS

1DF5  A60D     CRLF:     LDA      #ODH
1DF7  CD1F29   JSR      SEND

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LDA #0AH
JSR SEND
LDX #100

CRLF1: LDA #167 ;ABOUT A 10 MS DELAY
CRLF2: DECA ;INNER LOOP IS 1.001 MS
BNE CRLF2
DECX
BNE CRLF1

;SNDSTG SENDS STRING LOCATED ATXA TILL $ IS FOUND

1E0A B71F SNDSTG: STA PROG2+2
1EOC BF1E STX PROG2+1
1E0E A6C6 SNDST0: LDA #0C6H ;PUT LOAD INSTRUCTION IN PROG2
1E10 B71D STA PROG2
1E12 A681 LDA #81H ;PUT RETURN INSTRUCTION IN TOO
1E14 B720 STA PROG2+3
1E16 BD1D SNDST1: JSR PROG2 ;GET BYTE
1E18 3C1F INC PROG2+2 ;INCREMENT POINTER
1E1A 2602 BNE SNDST4 ;GET NEXT IF NO CARRY
1E1C 3C1E INC PROG2+1 ;INC REST OF POINTER IF CARRY
1E1E A124 SNDST4: CMP #'$'
1E20 2601 BNE SNDST2
1E22 81 RTS
1E23 A10A SNDST2: CMP #0AH ;SKIP LINE FEED
1E25 27EF BEQ SNDST1
1E27 A10D CMP #0DH ;DO CR WITH SUBROUTINE CRLF
1E29 2605 BNE SNDST3
1E2B CD1F5 JSR CRLF
1E2E 20E6 BRA SNDST1
1E30 CD1F29 SNDST3: JSR SEND
1E33 20E1 BRA SNDST1

INCAD: INC PROG1+2 ;INCREMENT ADDRESS POINTER
1E37 2602 BNE INCAD1
1E39 3C1A INC PROG1+1
1E3B 81 INCAD1: RTS

1E3C 3D1B DECAD: TST PROG1+2
1E3E 2602 BNE DECAD1
1E40 3A1A DEC PROG1+1
1E42 3A1B DECAD1: DEC PROG1+2 ;DECREMENT ADDRESS POINTER
1E44 81 RTS

1E45 AECC GOMEM: LDX #OCCH ;EXTENDED JMP
1E47 2006 BRA MEM
1E49 AEC7 PUTM: LDX #OC7H ;PREP FOR MOV M,A INSTRUCTION
1E4B 2002 BRA MEM
1E4D AE6C GETM: LDX #0C6H ;PUT LOAD INSTRUCTION IN PROG1
1E4F BF19 MEM: STX PROG1
1E51 AE81 LDX #81H ;PUT RETURN INSTRUCTION IN TOO
1E53 BF1C STX PROG1+3
1E55 BD19 JSR PROG1 ;AND PROG1+2
1E57 81 RTS

1E58 BE1A SAVAD: LDX PROG1+1
1E5A BF23 STX PROG4
1E5C BE1B LDX PROG1+2
1E5E BF24 STX PROG4+1
1E60 81 RTS

1E61 BE23 RECAD: LDX PROG4
1E63 BF1A STX PROG1+1
1E65 BE24 LDX PROG4+1
1E67 BF1B STX PROG1+2
1E69 81 RTS

;SNDAD SENDS ADDRESS IN PROG1+1 AND PROG1+2
;SNDBY SENDS BYTE IN A
;SNDNIB SENDS NIBBLE IN A

1E6A B61A SNDAD: LDA PROG1+1
1E6C CD1E75 JSR SNDBY
1E6F B61B LDA PROG1+2
1E71 CD1E75 JSR SNDBY
1E74 81 RTS

1E75 B716 SNDBY: STA TEMP3 ;KEEP COPY IN TEMP3
1E77 44 LSRA
1E78 44 LSRA
1E79 44 LSRA
1E7A 44 LSRA
1E7B CD1E84 JSR SNDNIB
1E7E B616 LDA TEMP3
1E80 CD1E84 JSR SNDNIB
1E83 81 RTS

1E84 A40F SNDNIB: AND #OFH ;GET 0-9 FIRST
1E86 AB30 ADD #'0'
1E88 A13A CMP #9+1
1E8A 2502 BCS SNDNII ;NOW LETTERS
1E8C AB07 ADD #'A'-9'-1
1E8E CD1F29 SNDNII: JSR SEND
1E91 81 RTS

;THIS SUBROUTINE GETS AN ADDRESS FROM THE TERMINAL
;ADDRESS IS IN PROG1+1 AND PROG1+2 AT COMPLETION
;NUMBER ROLLS OVER SO ONLY LAST 4 DIGITS ARE ACCEPTED
1E92 3F1A GETAD: CLR PROG1+1 ; 2- BYTE ACCUMULATOR
1E94 3F1B CLR PROG1+2 ; GETS DEFAULT ADDRESS OF 0
1E96 CD1EAC GETAD1: JSR GETNIB ; GET NIBBLE
1E99 5D TSTX ; LOOK FOR FLAG
1E9A 2601 BNE GETAD2
1E9C 81 RTS ; QUIT WHEN ZERO FLAG FOUND
1E9D AE04 GETAD2: LDX #4
1E9F 381B GETAD3: LSL PROG1+2 ; MAKE ROOM FOR NEW NIBBLE
1EA1 391A ROL PROG1+1
1EA3 5A DECK ; BY MOVING OVER 4 BITS
1EA4 26F9 BNE GETAD3
1EA6 BB1B ADD PROG1+2 ; ADD IN NEWCOMER
1EAA B71B STA PROG1+2
1EAC 20EA BRA GETAD1

1EAE CD1EFB GETNIB: JSR GET ; GET INCOMING CHARACTER
1EAF 97 TAX ; HIDE IT IN X
1EB0 A10D CMP #0DH ; LOOK FOR CARRIAGE RETURN
1EB2 272A BEQ GETN1
1EB4 A12E CMP #',.'
1EB6 260B BNE GETN2
1EB8 C6020B LDA 020BH
1EBB A47F AND #7FH ; CLEAR CLOCK SET BIT
1EBD C7020B STA 020BH ; IN CASE OF EXIT FROM CKSET
1EC0 CC1D32 JMP MONITR
1EC3 A030 GETN2: SUB #0'0'; LOOK FOR NUMBERS FIRST
1EC5 25E5 BCS GETNIB
1EC7 A10A CMP #10 ; DONE IF 0-9
1EC9 2508 BCS GETN3
1ECB A007 SUB #A'-9'-1 ; NOW LOOK FOR LETTERS
1ECD 25DD BCS GETNIB ; TRY AGAIN IF NOT A-F
1ECE A110 CMP #16
1ED1 24D9 BCC GETNIB
1ED3 B716 GETN3: STA TEMP3
1ED5 9F TXA ; MOVE NUMBER BACK
1ED6 CD1F29 JSR SEND
1ED9 B616 LDA TEMP3
1EDB AEFF LDX #OFFH ; CLEAR RETURN FLAG
1EED 81 RTS

1EE0 CD1EFE GETN1: CLRX ; RETURN FLAG
1EEF 81 RTS

1EE0 CD1EFE GETHX: JSR GETHX1 ; GET BYTE FROM TWO
1EE3 48 ASLA ; INCOMING CHARACTERS
1EE4 48 ASLA
1EE5 48 ASLA
1EE6 48 ASLA
1EE7 B718 STA TEMP5
1EE9 CD1EFE JSR GETHX1
1EEC BB18 ADD TEMP5

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1EEF 81 RTS
1EEF CD1E9B GETHXI: JSR GET ; GET HEX NUMBER FROM UART
1EF2 A030 SUB # '0' ; BYTE COMING IN IN ASCII
1EF4 A10A CMP # 10
1EF6 2502 BCS GETHX2
1EF8 A007 SUB # A' - '9' - 1
1EFA 81 GETHX2: RTS

******************* UART SUBROUTINES *******************

; ENTER OR EXIT WITH BYTE TO BE SENT IN ACCUMULATOR
; SENDS 7 BITS WITH NO PARITY
; RECEIVES ONLY 7 BITS
; WORKS WITH RATES 50 TO 9600 BAUD
; GET BRINGS CHARACTER IN FROM UART
; SEND SENDS CHARACTER OUT UART
; RASET SETS UART RATE

1EFB 0E01FD GET: BRSET 7, 1, GET ; WAIT FOR START BIT
1EFE BE10 LDX TIMA ; WAIT 1/2 BIT CELL
1F00 B611 LDA TIMB
1F02 57 ASRX
1F03 46 RORA ; DIVIDE BY 2
1F04 A005 SUB # 5 ; TIMING COMPENSATION
1F06 2501 BCS GET01
1F08 5C INCX
1F09 4C GET01: INCA
1F0A 4A GET02: DECA
1F0B 9D NOP
1F0C 26FC BNE GET02
1F0E 5A DECK
1F0F 26FB BNE GET02
1F11 AE80 LDX # 80H ; BIT IN D7 IS FLAG
1F13 CD1F55 GET3: JSR TIMIN3 ; 1 BIT CELL WAIT
1F16 54 LSRX ; MOVE OVER FOR NEXT BIT
1F17 250B BCS GET4
1F19 9D NOP
1F1A 9F TXA
1F1B 0F0102 BRCLR 7, 1, GET2 ; ADD NOTHING IF CLEAR
1F1E AB80 ADD # 80H ; PUT IN BIT IF NOT
1F20 97 GET2: TAX
1F21 9D NOP
1F22 20EF BRA GET3 ; QUIT WHEN ALL 7 DONE
1F24 CD1F4D GET4: JSR TIMIN1 ; WAIT ONE MORE CELL
1F27 9F TXA
1F28 81 GET6: RTS

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1F29 B715 SEND: STA TEMP2 ;SAVE CHARACTER
1F2B 1D01 BCLR 6,1 ;SET START BIT
1F2D AA80 ORA #80H ;LAST BIT FLAG
1F2F 97 TAX
1F30 CD1F55 SEND1: JSR TIMIN3 ;WAIT FOR TIMEOUT
1F33 54 LSRX ;GET NEXT BIT
1F34 270A BEQ SEND3 ;DONE IF ACCUMULATOR
1F36 2404 BCC SEND2 ;IS ZERO
1F38 1C01 BSET 6,1 ;SET TRANSMITTED BIT
1F3A 20F4 BRA SEND1
1F3C 1D01 SEND2: BCLR 6,1 ;CLEAR TRANSMITTED BIT
1F3E 20F0 BRA SEND1
1F40 1D01 SEND3: BCLR 6,1 ;FOR STOP BIT
1F42 CD1F51 JSR TIMIN2 ;WAIT FOR END OF STOP BIT
1F45 1C01 BSET 6,1
1F47 CD1F4D JSR TIMIN1
1F4A B615 LDA TEMP2 ;RECOVER CHARACTER
1F4C 81 RTS
1F4D A608 TIMIN1: LDA #8 ;BASIC TIMING ROUTINE
1F4F 2006 BRA TIMING
1F51 A609 TIMIN2: LDA #9
1F53 2002 BRA TIMING
1F55 A60A TIMIN3: LDA #10
1F57 B713 TIMING: STA TTIMB
1F59 B610 LDA TIMA
1F5B B712 STA TTIMA
1F5D B611 LDA TIMB
1F5F B013 SUB TTIMB
1F61 B713 STA TTIMB
1F63 2502 BCS TIMXX
1F65 3C12 TIMXY: INC TTIMA
1F67 3C13 TIMXX: INC TTIMB
1F69 3A13 TIMX: DEC TTIMB
1F6B 26FC BNE TIMX
1F6D 3A12 DEC TTIMA
1F6F 26F8 BNE TIMX
1F71 81 RTS
1F72 B610 TIMIN5: LDA TIMA
1F74 B712 STA TTIMA
1F76 B611 LDA TIMB
1F78 A00D SUB #13
1F7A B713 STA TTIMB
1F7C 2402 BCC TIMX1
1F7E 3A12 DEC TTIMA
1F80 3712 TIMX1: ASR TTIMA
1F82 3613 ROR TTIMB
1F84 20DF BRA TIMXY

;UART RATE SETTING ROUTINE: GOOD FOR 50 - 9600 BAUD
1F86 3F10      RATSET: CLR  TIMA  ;ZERO COUNTERS
1F88 3F11      CLR  TIMB
1F8A 0E01FD     RATS1: BRSET 7,1,RATS1  ;WAIT FOR INCOMING
1F8D           ;START BIT
1F98 3C11      RATS2: INC  TIMB
1F9F 2602      BNE  RATS4
1F91 3C10      INC  TIMA
1F93 5C        RATS4: INCX  ;IGNORED: CORRECTS TIMING
1F94 0F01F6     BRCLR 7,1,RATS2  ;WAIT FOR STOP BIT END
1F97           1F99 3910      RATS5: LSL  TIMB  ;IF SLOW RATE NEED NOT CORRECT
1F9B 2611      ROL  TIMA
1F9D B611      BNE  RATS7
1F9F 97        LDA  TIMB  ;CORRECT HIGHEST RATES
1FA0 A115      TAX
1FA2 2408      CMP  #21
1FA4 AE11      BCC  RATS6
1FA6 A10F      LDX  #17
1FA8 2402      CMP  #15  ;CORRECT 7200 & 9600 BAUD
1FAC AE0D      BCC  RATS6
1FEE BF11      LDX  #13
1FAB 81        RATS6: STX  TIMB  ;STASH IT IN SAFE HIDDING
1FAE 81        RATS7: RTS

;INTERRUPT AND RESET VECTORS.

1FF6            ORG 1FF6H
1FF6 1B00       DB  1BH,00H  ;HIGH,LOW WAIT TIMER
1FF8 1B03       DB  1BH,03H  ;HIGH,LOW TIMER INT
1FFA 1840       DB  18H,40H  ;HIGH,LOW HARDWARE INT
1FFC 1809       DB  18H,09H  ;HIGH,LOW SOFTWARE INT
1FFE 1800       DB  18H,00H  ;ROM START FROM RESET
0000           END

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An FSK Telemetry Module for Vector Measuring Current Meters

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The EG&G Vector Measuring Current Meter (VMCM) used in mooring work provides a 20 ma Serial ASCII Instrumentation Loop (SAIL) communication system. A projected application of the VMCM is to have a surface mooring communicate with a series of VMCMs via a Frequency Shift Keying (FSK) link. While an FSK modem can communicate with the VMCM, a problem exists with the general operation of the VMCM. If the VMCM is addressed to dump data, it remains on until the unit is re-addressed. If a failure in the link occurs, then the VMCM stays on in a higher power mode and the batteries will be depleted early.

The insertion of a processing block between the modem and the VMCM provides a way to look at incoming data, qualify it and re-transmit it to the VMCM. The VMCM will reply and the preprocessor can channel the data to the modem. In the event of a VMCM malfunction, the preprocessor has a timeout function and will turn off the carrier keeping the line quiet.

1. Vector Measuring Current Meter
2. FSK SAIL Communications
3. Telemetry Buoy