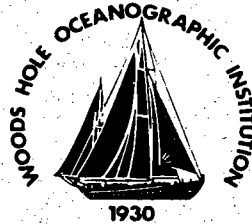


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**A SAIL Compatible Three Channel
Acoustic Navigation Interrogator**

by

Stephen P. Liberatore

September 1990

Funding was provided by the Office of Naval Research
under Contract Nos. N00014-82-C-0152 and N00014-85-C-0379.

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Stephen P. Liberatore

Woods Hole Oceanographic Institution
Woods Hole, Massachusetts 02543

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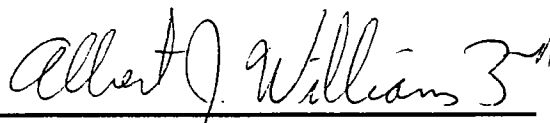
Technical Report

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Department of Applied Ocean Physics & Engineering



ABSTRACT

Ocean Acoustic Tomography data are significantly degraded if mooring motion is unknown. An autonomous instrument employing a solid state data logger designed to track and record mooring motion is described.

Navigation is accomplished by simultaneously interrogating each of three bottom mounted transponders positioned in an equilateral triangle around the mooring's anchor at a range approximately equal to the depth of the tracked instrument. The three round-trip travel times thus obtained having a resolution of 125 μ S and a SNR dependent jitter of less than 1.5mS, define a unique instrument position and are recorded along with the time of day and day of year.

The measurement period, the system clock and the program start time are set via a 20mA SAIL. Since the standby power requirement is negligible compared to the battery capacity, the instrument may be programmed months in advance of the deployment.

System endurance varies with the measurement period, however, typical programs permit navigation for up to 21 months at 12 points per day.

Upon recovery, the navigator data may be down-loaded via SAIL directly to the storage medium of a suitable computer.

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1.0 GENERAL DESCRIPTION

1.1 Introduction

The requirement to spatially track acoustic transceivers moored as part of an Ocean Acoustic Tomography experiment has led the Woods Hole Oceanographic Institution and Benthos Inc. of Falmouth, Ma, to develop an acoustic mooring navigation system.

The electronics module designed at W.H.O.I. and described in this manual is used with the BENTHOS model (ES) 210-TCSSA acoustic transceiver. Together they form a Mooring Motion Monitoring Module (QUAD M) Interrogator.

This document serves as a system hardware reference manual for the technical, but uninitiated user. It references other hardware manuals where appropriate and provides system-oriented information unavailable elsewhere. A copy of the interrogator control program (PNAVLGR) is included as an addendum to this manual.

1.2 System Components

Tracking is accomplished by measuring round-trip travel time from the interrogator to three transponders. The transponders are moored about three meters above the ocean floor and approximately one water depth away from the mooring anchor.

Figure 1 is a block diagram of a mooring equipped to monitor the motion of an instrument mounted near a sub-surface float. "A", "B", and "C", are bottom-mounted acoustic transponders, either Benthos model 210-TR17A-GF which are recoverable or model XT-6000 which are not. The interrogator is mounted as near as practical to the instrument tracked. The frequencies depicted are those which were originally employed. To remain compatible with as many tomography instruments as possible, the 13.5kHz channel has been returned to 12.0kHz.

The interrogator pings to all three transponders simultaneously at a predetermined time and at a predetermined rate. The time required to receive a response from each transponder, along with the time of day and date, are stored in CMOS static RAM.

The operating parameters are set via the Serial ASCII Instrumentation Loop (SAIL). Pre-deployment checks and data retrieval are also accomplished over the SAIL. A formal description of the SAIL standard is presented in U.N.O.L.S. Ref. TAC-81-1 Aug. 1981, "Serial ASCII Instrumentation Loop (SAIL)" or IEEE standard 997-1985.

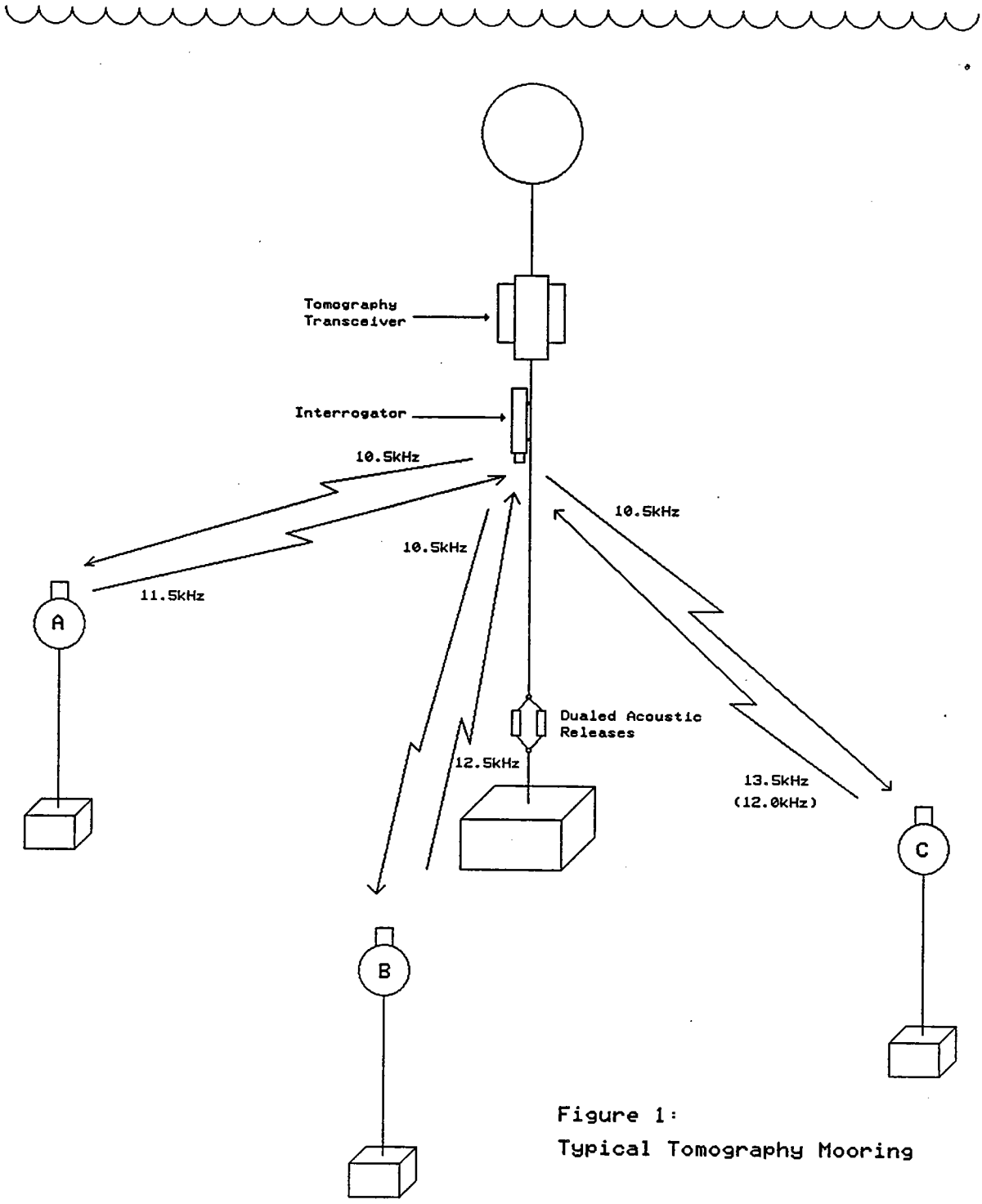


Figure 1:
Typical Tomography Mooring

2.0 SPECIFICATIONS

2.1 Interrogator

The transceiver specifications, except the electrical power source and operating life, are as listed in the Benthos operating manual for the (ES)210-TCSSA. These two exceptions are the result of replacing a MICRO tape recorder and its associated control electronics with a solid state memory and a power-switched, microprocessor-based controller. The transceiver configured in this manner will henceforth be referred to as an interrogator.

2.2 Power

Twenty-one 1.5 volt "D" size alkaline cells supply power for the interrogator. The DURACELL B1300-T2, with spot welded solder tabs on both terminals is the preferred cell.

The cells are configured as follows: Two diode-isolated parallel strings, each consisting of 9 cells are wired in series yielding 12 volts, then 3 cells are wired in series with the 12 volt stack to yield 16 volts. The battery thus formed is tapped at 12 volts to power the acoustic receiver and the digital electronics, while the 16 volt tap supplies the pinger's power amplifier.

De-rating for temperature and storage, and assuming an average cell voltage of 1 volt, each cell will yield approximately 10 watt hours. The above stack is therefore rated at 210 watt hours.

Making one measurement per hour, the interrogator requires fewer than 0.0045 watt hours. This yields an operating life in excess of 5 years, which exceeds the nominal self discharge time of an alkaline cell. It is however, recommended that the battery be replaced before each deployment.

2.3 Schedule

A measurement may be made as often as every three minutes, or as seldom as once every 999 minutes. The time-of-day clock must be set to the nearest whole minute. Assuming that the clock's oscillator was adjusted to 32.768kHz with the interrogator at the same temperature encountered while deployed, its time will be accurate to within +/- 5 minutes after 365 days, i.e., the clock will lose or gain about 1 second per day. The start of a measurement sequence may be scheduled on any whole minute of the year. Leap years are not accounted for so the clock will reset to day 1 on day 366 of a leap year. **Note:** Interrogator S/N 005 has an alternate program allowing it to make measurements as often as every 3 seconds or as seldom as every 999 seconds. This system is typically employed as a recording acoustic range finder for towed instruments.

2.4 Data Format

The 60K RAM (Random Access Memory) allows space for 7648 measurements which, at 12 measurements per day, yields a system endurance in excess of twenty months. After the 7649th

measurement, which will be made but not stored, the system will enter the "idle" mode, and no further measurements will be made.

Each measurement consists of a 16 bit time-of-day word, and three 16 bit two-way travel time words. The time of day is recorded with a resolution of one hour. An LSB of travel time is equal to 250 uS. Measurement data, stored beginning at RAM address 1000H, are ordered as follows:

Time of day, Travel time A, Travel time B, and Travel time C.

The time of day is encoded as follows:

BIT #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNITS	HD	HD	TD	TD	TD	TD	UD	UD	UD	UD	TH	TH	UH	UH	UH	UH
WEIGHT	2	1	8	4	2	1	8	4	2	1	2	1	8	4	2	1

Where HD is hundreds of days, TD is tens of days, UD is units of days, TH is tens of hours, and UH is units of hours.

As an example, a time code word of 11D6H would convert to day 047 hour 16 as follows:

1	1	D	6
00	0100	0111	01 0110
HD	TD	UD	TH UH
0	4	7	1 6

2.5 Transponder

The transponder specifications may be found in BENTHOS report 0-210-TR17A-GF or the XT-6000 Technical Manual.

3.0 OPERATION

3.1 Power On / Reset

Following the instructions in Benthos manual 0-210-TCSSA, section 2.1, remove the electronics from the pressure housing. Position the electronics with the back-plane wiring facing away from you and with the transducer on your left. Locate the power switch near the transducer end of the instrument and ensure that it is in the "on" position. Locate the reset pins on the opposite end of the instrument and short them together for at least five seconds. This will reset the digital electronics and start the microprocessor.

3.2 Connect to SAIL

Connect to the SAIL via the banana jacks on the controller electronics card. Insure that the loop is closed and connect a terminal to the SAIL / RS-232 converter. Set the terminal for seven data bits, even parity, 1 stop bit, and 300 baud.

3.3 Monitor Current

Connect a digital voltmeter between test points 1 and 2 which are located on either side of R1 on the System Control card. The meter will read total system current scaled at 100uA/mV.

Once the SAIL loop is closed and a full minute has elapsed, the voltmeter will read between 60 and 80 mV. If less than a minute has elapsed the reading may be between .3 and .6 mV. **Wait for the higher reading** which indicates that the processor is awake and ready for SAIL control.

Note: Most of the interrogators are now equipped with a LED to monitor the switched power. With these instruments there is no need to monitor the voltage across R1. Simply wait for the LED to light before attempting to address the interrogator.

3.4 Address

Once the microprocessor has detected the presence of a closed SAIL and applied power to the rest of the system, the instrument may be addressed by typing **#In** where n is the interrogator's serial number. A correctly addressed instrument will respond with:

In READY

:

EXAMPLE

```
#I3 <--- You type this line
I3 READY <--- Interrogator
: <--- reply
```

The ":" in the above example is the system prompt and signifies that the interrogator is awaiting commands. Type an H and the interrogator will print a list of the available commands.

EXAMPLE

: H

INTERROGATOR PROGRAM Ver. 1.1 Jan. 1985

SYSTEM COMMANDS

!Maaaa dddd	LOAD MEMORY
?M	DISPLAY MEMORY
?Paaaa	RUN PROGRAM
?C	CALCULATE CRC
M	MOVE MEMORY
R	TEST RAM
?S	DISPLAY SCHEDULE
!SCHEDULE	PROGRAM SCHEDULE
!TIME	SET CLOCK
?T	DISPLAY TIME
!LOCK	PROTECT MEMORY
!UNLOCK	UNPROTECT MEMORY
!IDLE	INHIBIT SCHEDULER
!PING	TRANSMIT A 10mS PULSE

3.5 Entering Commands

To initiate a command, simply type it exactly as it is listed in the "HELP" file. An error message will be printed in response to an unrecognized command. Usually this message will be followed by the "prompt", at which time you may try re-entering the command. **NOTE: Commands are NOT terminated with a "Carriage**

Return", but ALL numeric entries in response to system prompts MUST be terminated with a "Space".

3.6 Correcting Errors

Numeric entries are expected to be a certain number of digits in length. For example, when entering the start hour, a two digit figure is expected; but when entering the measurement interval, a three digit figure is expected. **Only the last n digits typed prior to a "Space" are entered** (n is the number of digits expected). Because of this, typing errors may be corrected by simply typing the correct figure immediately after the error. For example, when entering the measurement interval, if you mistakenly type 20 when what you really wanted was 120, the corrected entry would look like this: 20120. Similarly, an hour entry of 2314234121 would be accepted as hour 21.

3.7 PROM Test

Test the system program memory by typing ?C and answering the questions with 0 over 800, and 800 over 800. Verify the correct response by comparing the calculated CRC with the values recorded on the PROMS, IC 4 and 5.

```
EXAMPLE      : ?CRC From 000 Over 800 = 994C
              : ?CRC From 800 Over 800 = EF9A
              :
```

3.8 RAM Test

Test the system RAM by typing **!UNLOCK**. The system will respond with OK. Then type an R. The system will respond by typing a cosmetic "am" and the words "Test From". You answer with **1000**, and the system will then type Over, to which you answer **F000**. A RAM test over this much memory requires about one minute and seven seconds. After each successful pass, the system will type a *. Ten such passes would indicate good memory. Reset and address the system as in **3.1** and **3.4** respectively.

```
EXAMPLE      : !UNLOCK OK
              : Ram Test From 1000 Over F000 OK (Y/N) ? Y
*****
```

The **!UNLOCK** command is required since RAM test will overwrite any measurements previously stored. The program will automatically execute the **!LOCK** command when the RAM test is terminated.

3.9 Clock Set

Set the system clock by typing **!TIME DDD HH MM 00** where DDD is the year day, HH is hours and MM is minutes. Since the interrogator clock has a one minute resolution, seconds must always be entered as 00 and the clock must be started on the minute. When real time is equal to the time entered, type an @. This will start the clock. To verify that the correct time was entered and that the clock is running, re-address the instrument (Section 3.4) and after the prompt, type ?T. The interrogator will

respond with the current time plus one minute, wait for the real time to equal the time just printed and, on the mark, printing an @.

```
EXAMPLE          !TIME 123 21 35 00 @
                  #In
                  #In READY
                  : ?T 123 21:36 00 Z...@
                  :
```

3.10 Schedule

Set the operating schedule by typing **!SCHEDULE**. The Interrogator will ask you for Start day, hour, minute, and the measurement interval. Terminate all entries with a **SPACE**. When all parameters have been entered, the interrogator will ask permission before activating the scheduler.

```
EXAMPLE  : !SCHEDULE
          Start on day = 115   Hour = 18   Minute = 30
          Measurement interval, minutes = 060   OK (Y/N) ? Y
```

3.11 Verify Schedule

Verify that the schedule has been accepted as entered by typing **?S**. The interrogator will respond by typing the current time and schedule in addition to the system status (ARMED, not ARMED, or ACTIVE). If the system is ACTIVE, the number of minutes remaining to the next measurement (in HEX) and the current data

address pointer will also be shown.

EXAMPLE : ?S

At 115 18:10
Start on day = 115 hour = 18 minute = 30
Measurement interval = 060 minutes
Scheduler is ARMED BUT NOT ACTIVE

3.12 Test Pinger

Test the pinger by typing **!PING**. The interrogator will respond by typing OK (Y/N) ? If you next type a Y you should hear the transmit pulse.

EXAMPLE : !PING OK (Y/N) Y
:

3.13 Final Test

Disconnect the SAIL cable and observe the system current immediately drop to some value below 100uA. At the next one minute mark, the current will rise to a level near 7mA and stay at that level for about 70mS. If the interrogator is equipped with a LED, it will dimly flash. These observations indicate that the interrogator is functioning correctly and the instrument may be encased in its pressure housing. Refer to section 2.1 of

BENTHOS manual (ES) 210-TCSSA and, following instructions there, place the electronics within the pressure housing. At this point the interrogator is ready for deployment.

3.14 Data Recovery (fast)

When the instrument is recovered, the data which are stored in RAM may be down loaded at a high baud rate directly to the storage medium of a suitably equipped computer. **Be careful not to interrupt power to the system in any way as this WILL result in lost data.** Proceed as follows:

- a. Remove the electronics from the pressure housing (3.1)
- b. Connect the SAIL to RS-232 converter box. (3.2)
- c. Monitor current, and wait for the high reading. (3.3)
- d. Replace the jumper plug located on the control card (P3) with the cable from the 5 VOLT BAUD RATE GENERATOR. Set the baud rate generator for 9600 baud. (see Figure 8.)
- e. Connect the auxiliary I/O port of the computer to the RS-232 connector on the SAIL to RS-232 converter.
- f. Set this port for 9600 baud, seven data bits, one stop bit, and even parity.

- g. Using the computer terminal (and the appropriate communications program) address the interrogator. (3.4) .
- h. Type ?S to verify that the system is still "ACTIVE", that the clock is still running, and to obtain the data address pointer. Subtract 1000H from the current address pointer, and make note of the result.
- i. Type !IDLE to inhibit further measurements.
- j. Prepare the computer to receive an ASCII data file, and type ?M. The system will respond by printing From. You respond by typing 1000. The system will then print Over, and you respond by typing the result of the calculation done in 3.14 (h.) followed by a carriage return.

The interrogator down loads two measurements per line. A full memory (7648 measurements) requires approximately three minutes to down load.

4.0 THEORY OF OPERATION

4.1 Acoustic Electronics

Section 5 of Benthos report O-210-TCSSA explains the operation of the acoustic electronics.

4.2 Power Supply

Refer to Figure 2, which is a simplified block diagram of the interrogator. The capacitor board, the 5 volt regulator, and the low voltage detector are the only blocks which receive power directly from the battery. The 5 volt regulator supplies power on a continuous basis to two other blocks, the clock, and the 60K CMOS static RAM. All other blocks are powered intermittently.

Refer to Figure 3, which is a schematic drawing of the interrogator power supply. These components are located on the SYSTEM CONTROL PC card. R1 is in series with the 12 volt stack, and is used as a current sense resistor for the entire electronics package. A voltmeter placed across this resistor will display current scaled at 100 uA/mV. The ICL 7663 is a micro-power voltage regulator with over-current sense. The output of this regulator is set to 5.5 volts by adjusting P1. The 2N3643 is a series pass transistor used to supply surge current during the power-up sequence.

The ICL7665 is a micro-power under voltage detector. Its

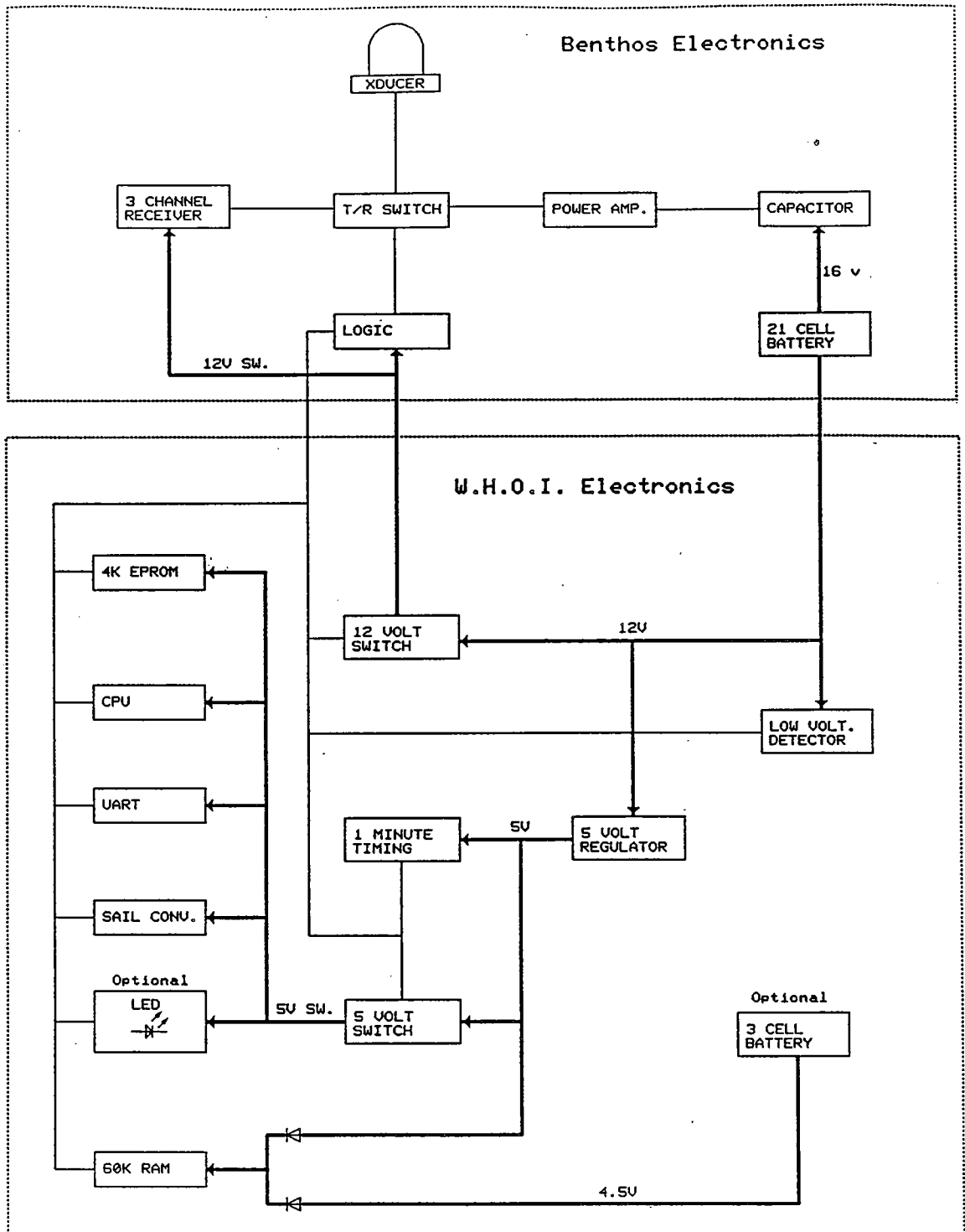


Figure: 2 Interrogator Block Diagram

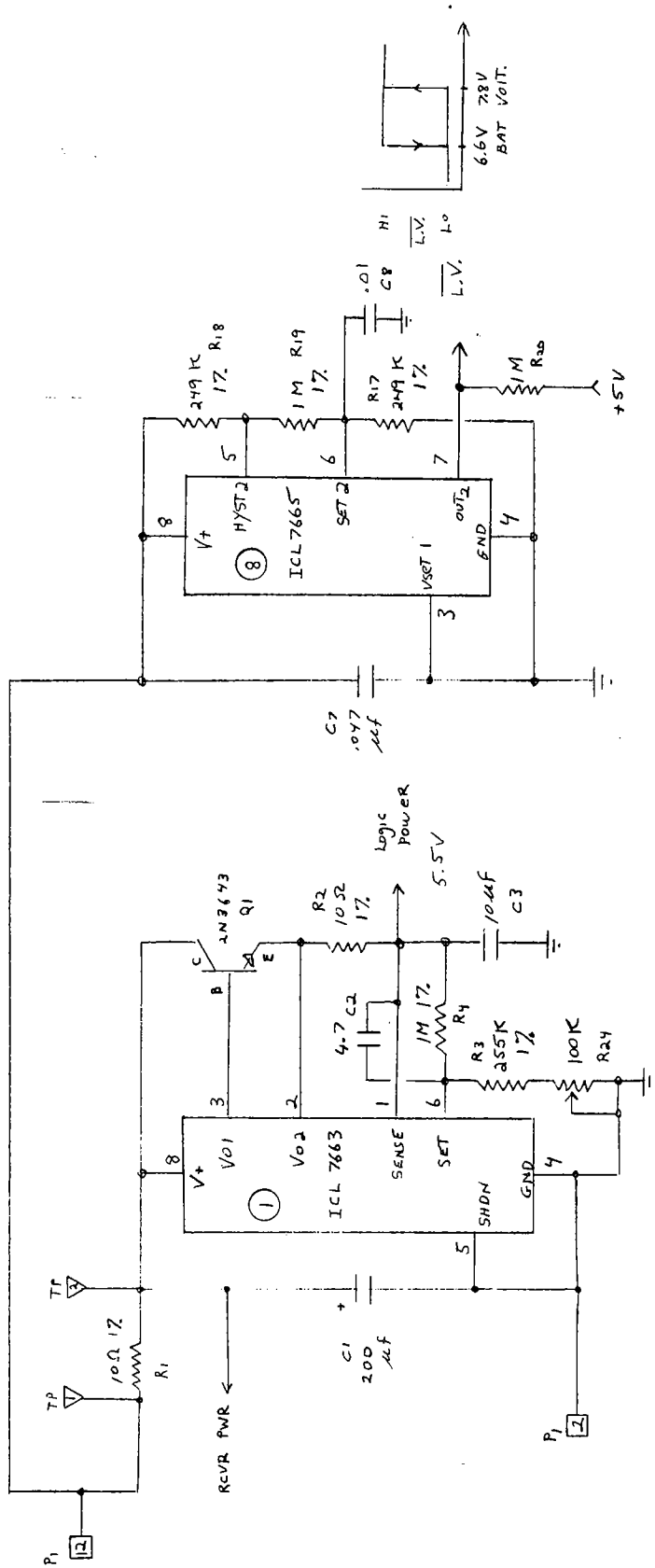


Figure 3: Interrogator Power Supply Schematic

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TITLE INTERROGATOR POWER SUPPLY
 FIG. 3

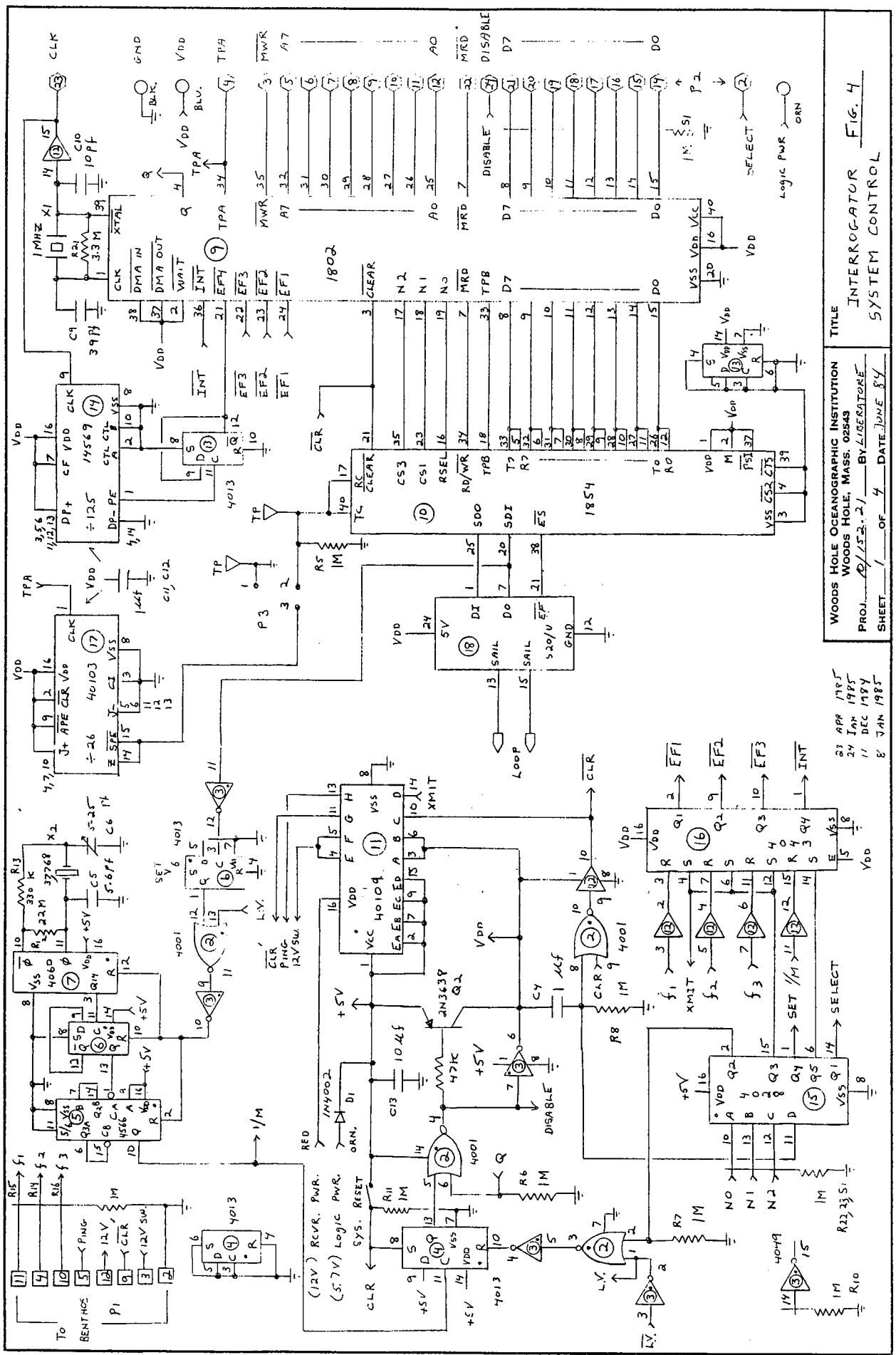
purpose is to monitor the battery and at a preset voltage inhibit further measurements in order to conserve battery power for data retention. When the battery voltage drops below 6.6 volts, LV NOT goes true (logic 0). This will stop a measurement in progress, and inhibit any further measurements from being initiated. LV NOT will remain true until the input voltage on P1-12 rises above 7.8 volts. The 1.2 volt hysteresis prevents the switch from oscillating between true and false, which could occur due to the difference between the open circuit voltage of the battery and the battery voltage while the system is enabled.

4.3 System Control

Refer to Figure 4. This is a schematic of the interrogator system control. These components are located on the same card as the power supply. 5 volt logic power enters through diode D1. This diode drops approximately .5 volts so that VCC and VDD to all components on this card will equal about 5 volts. If this is not the case, check the adjustment of R24.

IC 5,6, and 7 provide a once-per-minute pulse. If the rest of the system is already powered, this pulse simply generates an interrupt for the microprocessor (IC9). If the rest of the system was not already powered, the once-per-minute pulse will clock a HIGH to pin 13 of IC 4. This causes pin 4 of IC 2 to go LOW which enables system memory and turns on Q2.

VDD is applied to the remaining unpowered ICs on this card when Q2 is on. IC 11, which was already powered, now has VDD on input pins 3 and 6. VDD is level shifted via this IC to 12 volts and fed through P1 directly to the BENTHOS electronics.



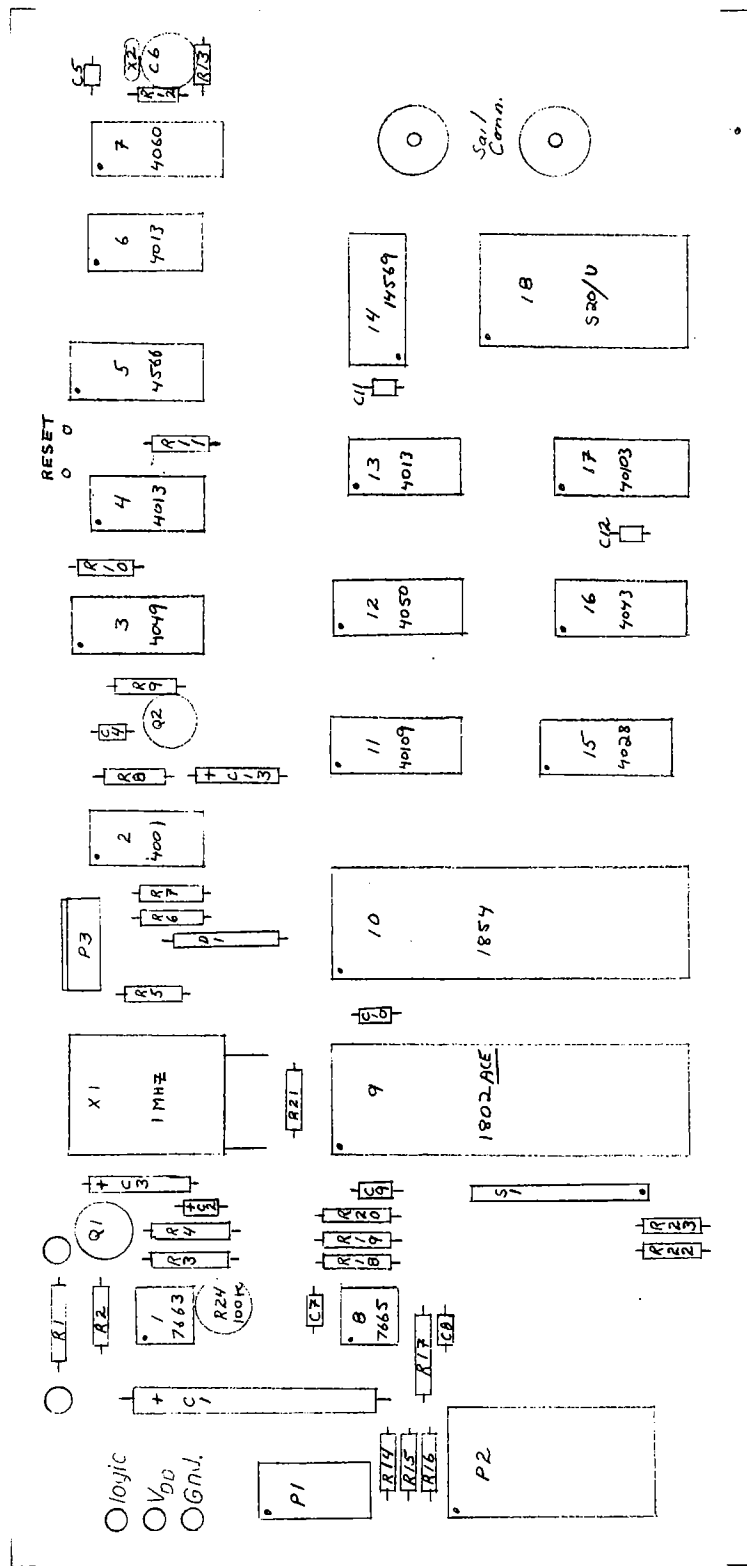
TITLE INTERROGATOR FIG. 4
 SYSTEM CONTROL

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 SHEET 1 OF 4 DATE JUNE 84

23 APR 1985
 24 JAN 1985
 11 DEC 1984
 8 JAN 1985

Figure 4: Interrogator System Control Schematic
 23

Figure 4a: Interrogator System Control Component Location



Assembly Notes

Install C2 before C3
 Q1 must be offset to the left to allow for C3
 Use turret terminals for first pinouts and power connections
 Secure X2 to C5 with small amount of RTV

When VDD first goes high, a reset pulse is generated via C4 charging through R8. The reset pulse is applied directly to pin 11 of IC 15 which inhibits this IC and prevents inadvertent I/O operations. The reset pulse is also inverted via IC 2 and 12. The inverted reset (CLR NOT) is level shifted via IC 11 and routed to the BENTHOS transmitter through P1. This signal, along with a slight modification to the BENTHOS electronics, prevents the transmitter from pinging upon power up. CLR NOT is also connected to IC 9 and 10. IC 9 is the microprocessor, and when CLR NOT goes HIGH, program execution begins at address 0000. The software clock is updated once the program has been initialized, and the UART (IC 10) is examined to determine if the SAIL is open or closed. If the loop is found to be open, a test is made to determine if it is time to begin a measurement cycle. If the loop is closed, interrupts are enabled and take over the function of updating the clock. If the loop is open and it is not time to begin a measurement the microprocessor generates a signal which appears on IC 15 pin 2. This signal is then gated to the reset pin of IC 4 via the OR gate composed of IC 2 and 3. Resetting IC 4 causes a HIGH to appear on pin 4 of IC 2 which will disable the memory select circuits and cause Q2 to turn off. The disable signal is inverted by IC 3, and the LOW thus produced is connected to VDD. Since Q2 is no longer conducting, this LOW will cause VDD to drop rapidly.

NOTE: It is important to remember that the microprocessor reacts to a manual reset in exactly the same fashion that it reacts to the once-per-minute tick. **For this reason, the interrogator clock, which resides only in software, will be advanced one minute with each manual reset, regardless of how much time has actually elapsed.**

IC 14 and 13 divide the 1MHz clock by 250 to produce a 4 kHz square wave which is applied to pin 21 of IC 9. During a measurement sequence, the microprocessor will increment three separate counters on each rising edge of this signal. The action begins immediately after a ping is transmitted, and continues until either all three transponders reply or the counters overflow. The reply detected signals (f1, f2, and f3) from the BENTHOS electronics enter through P1, are level shifted by IC 12, and latched by IC 16. The output of the latch is connected to pins 22, 23, and 24 of the microprocessor; these are three of the flag lines. When the microprocessor detects one of these flags, it stops incrementing the counter associated with that reply channel. The number remaining in the counter represents the two-way travel time. A counter which contains all zeros has overflowed and indicates no reply on that channel.

IC 18 converts the 20 mA SAIL levels to 5 volt CMOS levels for the UART, and provides an output which indicates an open loop. IC 17 divides the TPA clock signal from IC 9 by 26 to provide the 16X clock rate the UART requires to run at 300 baud.

The Q4 output of IC 15 and the D0 output of IC 18 synchronize the clock. Once the time has been entered, the microprocessor generates a signal which causes Q4 of IC 15 to go HIGH. This is the SET signal and is applied to the set input of IC 6. Pin 1 of this IC goes HIGH and is gated by the OR gate formed with IC 2 and 3 to the reset inputs of IC 5, 6, 7. This stops the clock's oscillator and resets its down counters. The start bit of any character typed over the loop will be inverted by IC 3 and used to clock IC 6. This will remove the reset and allow the clock's oscillator and down counters to operate. If the character was not an "@", the microprocessor will again

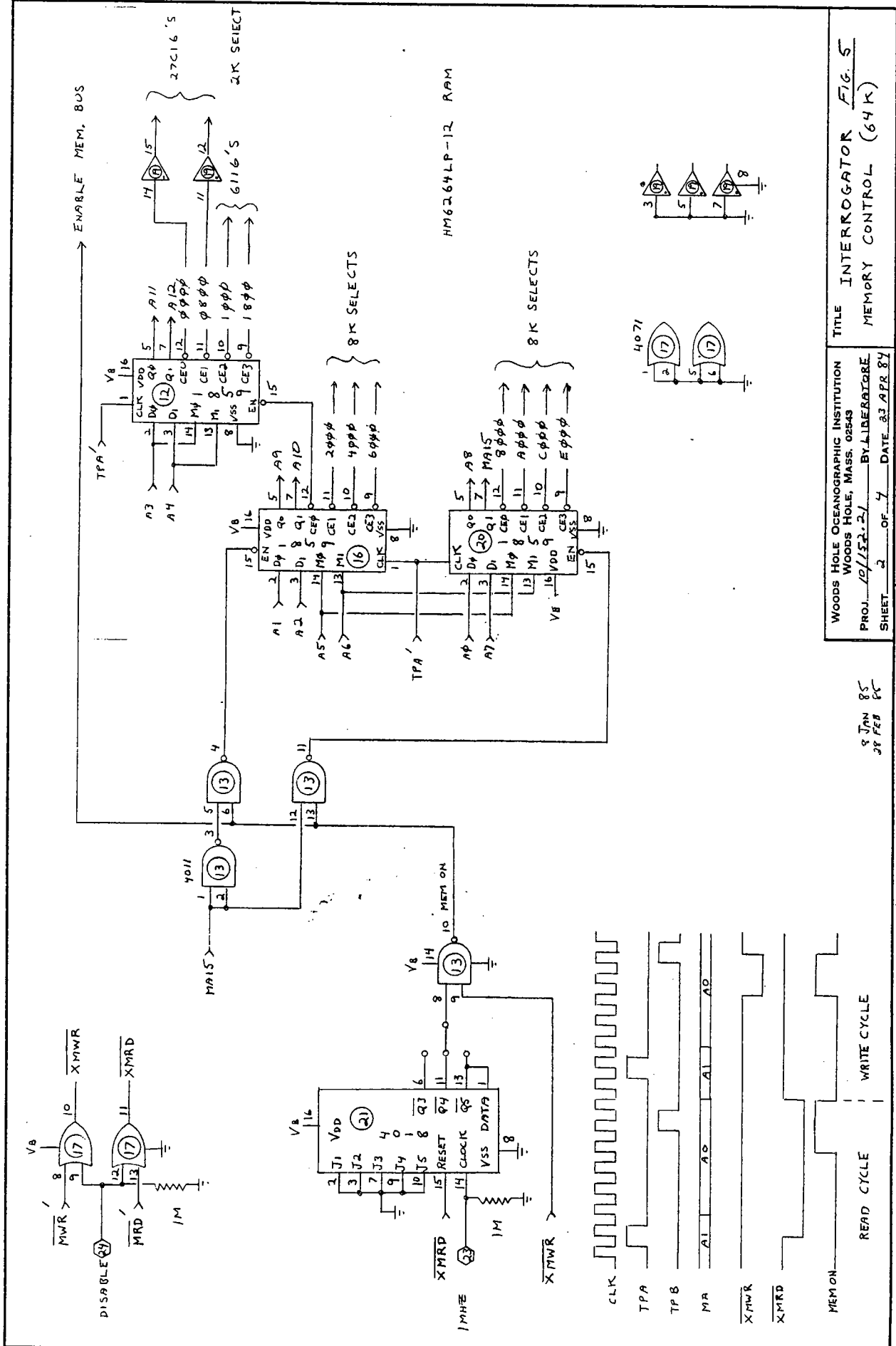
generate the signal which causes Q4 of IC 15 to go HIGH, and the cycle repeats.

4.4 Memory Control

Refer to Figure 5. This is a schematic of the memory control electronics. These components are located on the 64K memory card.

IC 17 gates the buffered MWR NOT and MRD NOT signals with the DISABLE signal generated on the system control card. This signal will go true just before power is removed from the microprocessor. When disable is true, both XMWR NOT and XMRD NOT are false (logic "1"). XMRD NOT being HIGH holds IC 21 reset. The Q4 output of IC 21 is applied to pin 8 of IC 13; and since pin 9 of this IC is also HIGH, its output, pin 10, is LOW. This is the memory on (or enable memory bus) signal, and when LOW, inhibits all memory operations by de-selecting the memory chips and by turning off the memory bus drivers.

IC 16, 18, and the remaining NAND gates of IC 13 decode the address lines to produce the 8K selects which enable the HM6264 RAM chips on this card. IC 12 decodes the proper address lines to produce the 2K selects which are required by the 27C16 PROM chips, and the HM6116 RAM chips. Since the PROM is power switched, the 2K selects used by these chips are buffered by IC 19. IC 21 is a counter and, with IC 13, is used to truncate the memory cycle and thus conserve power. **It is recommended that the jumper from pin 8 of IC 13 to pin 11 of IC 21 be moved to pin 13 of IC 21, thereby increasing the memory enabled time by 1uS.** This modification, although not essential and causing a slight increase in power consumption, will improve the system's reliability.



TITLE INTERROGATOR FIG. 5
 MEMORY CONTROL (64K)
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 38 FEB 85

Figure 5: Interrogator Memory Control (64K) Schematic

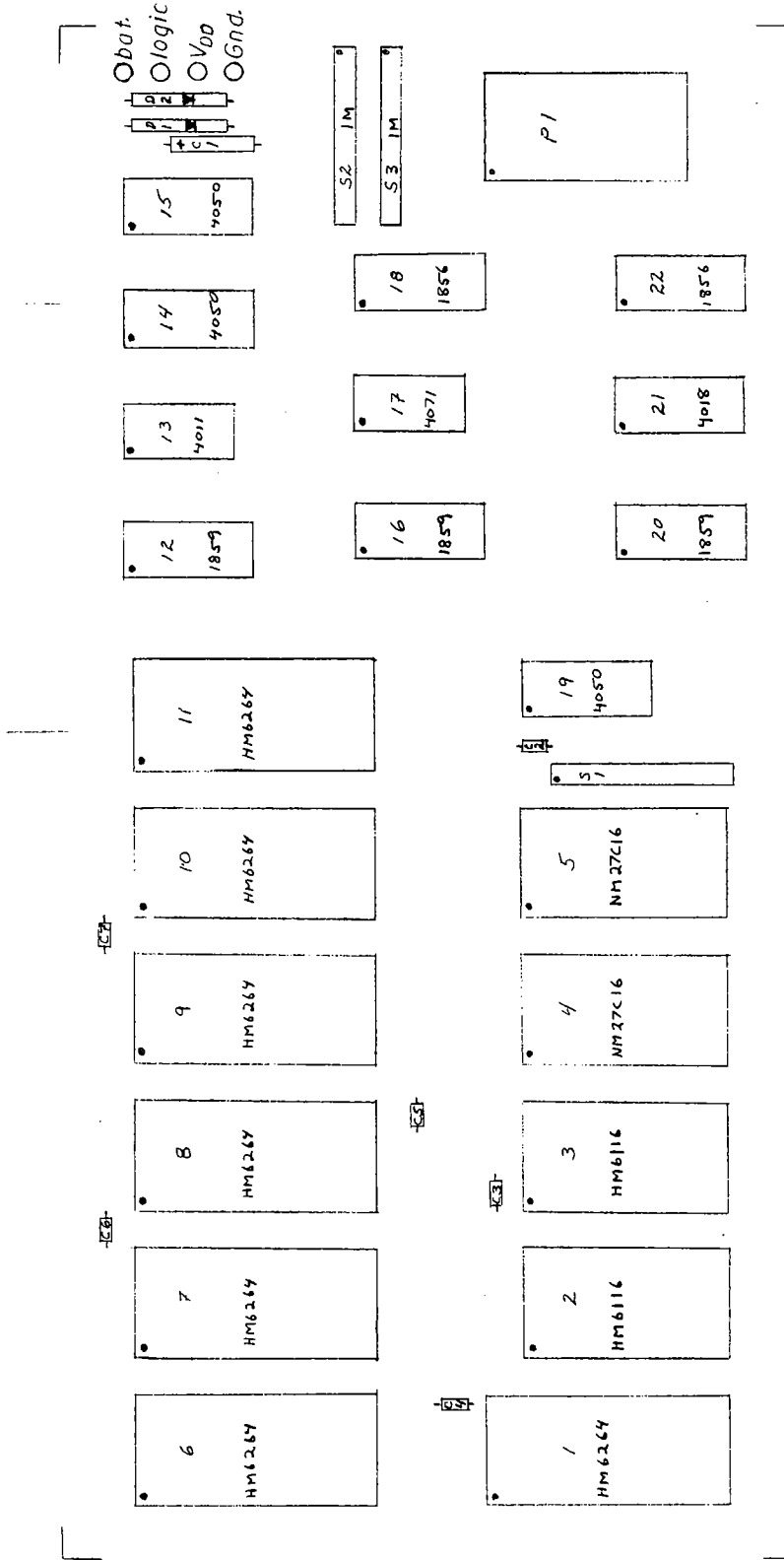
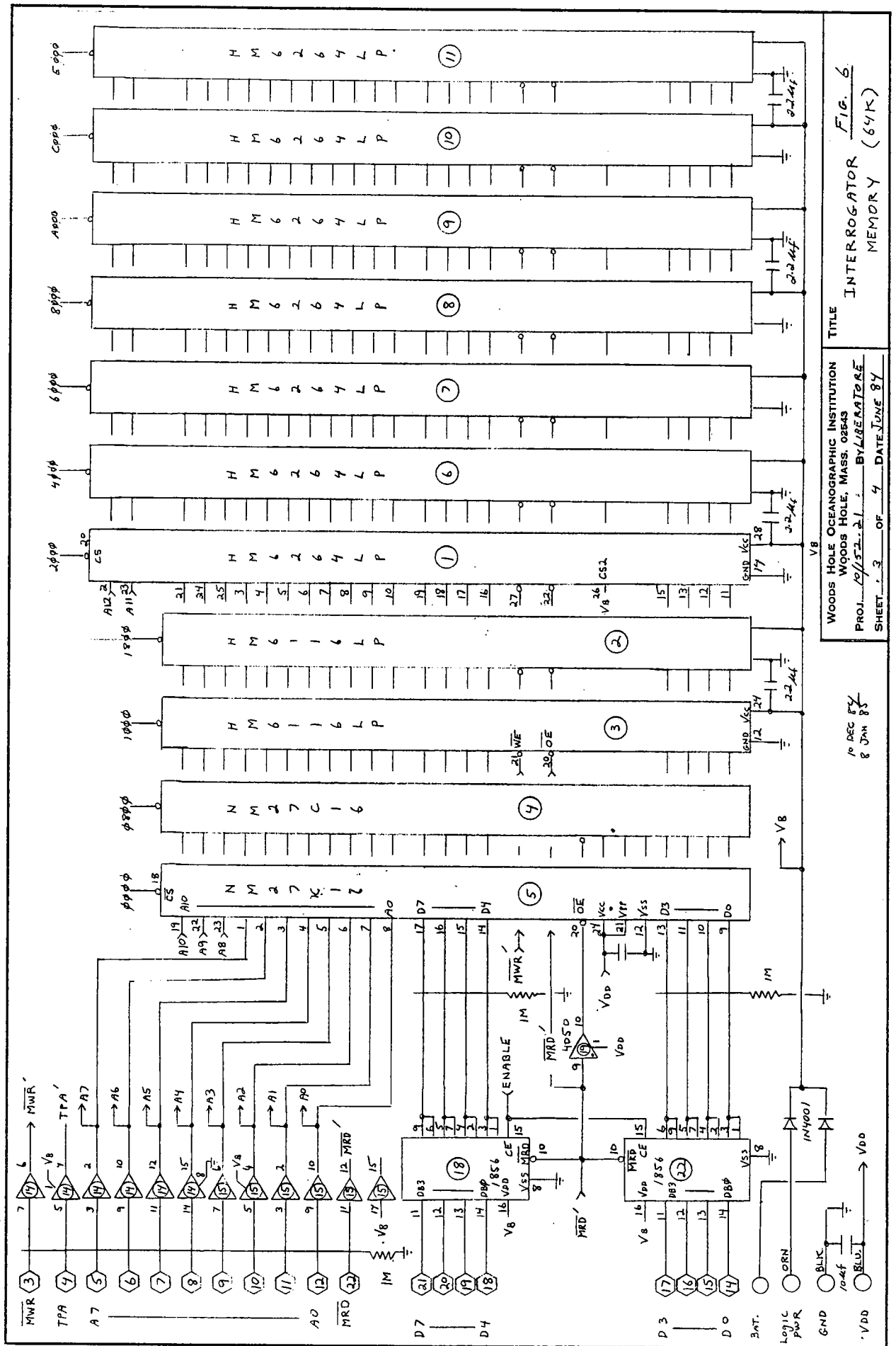


Figure 5a: Interrogator Memory (64K)
Component Location

4.5 64K Memory

Refer to Figure 6. This is a schematic of the system memory. These components are located on the same card as the memory control electronics. A 24 pin ribbon cable connects the memory card to the system control card. The memory is fully buffered by IC 18 and 22 which buffer the data lines and IC 14 and 15 which buffer the address and clock lines. Since IC 4 and 5 are power switched the MRD NOT signal is buffered by IC 19.

Power for this card is supplied via a disconnect through two diodes which isolate the logic power from the memory back-up battery. The back-up battery is composed of three AAA cells wired in series and, if used, is mounted on the rail over the system control card.



TITLE INTERROGATOR MEMORY (64K) FIG. 6
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10 DEC 87
 8 JUN 88

Figure 6: Interrogator Memory (64K) Schematic

5.0 MODIFIED BENTHOS ELECTRONICS

Slight modifications were made to the electronics supplied by BENTHOS. The effects of these modifications are as follows:

- a. A six-volt tap from the battery stack is eliminated.
- b. Transmitting on every power-up sequence is prevented.

5.1 Logic Board

Refer to BENTHOS drawing B-210-248. This is a schematic for the LOGIC board which must be modified to make provision for a power-up reset pulse. The power-up reset pulse originates on the system control card and inhibits the pinger during the power on cycles which occur at the rate of one per minute. Remove the LOGIC board from the chassis and locate IC 2, a CD4098B. Remove the etch between pins 3, 16, and 13 of IC 2. Connect pin 13 to pin 16 with a short jumper. Connect pin 3 to board I/O pin 10 with another short jumper. Clean the board of flux, and re-coat the patched area with a clear acrylic.

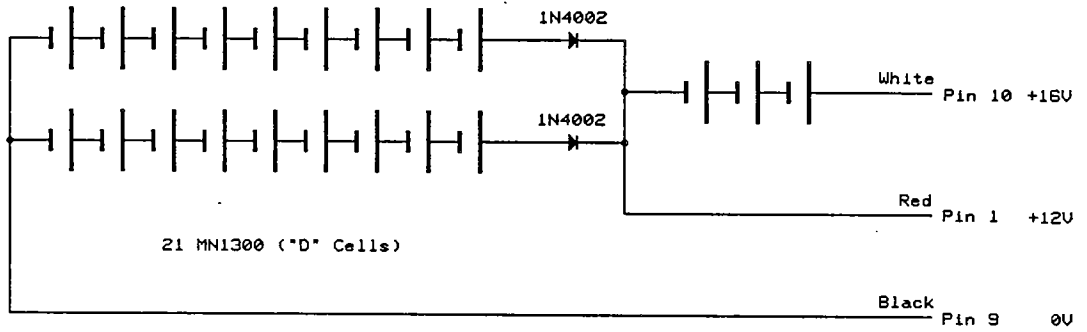
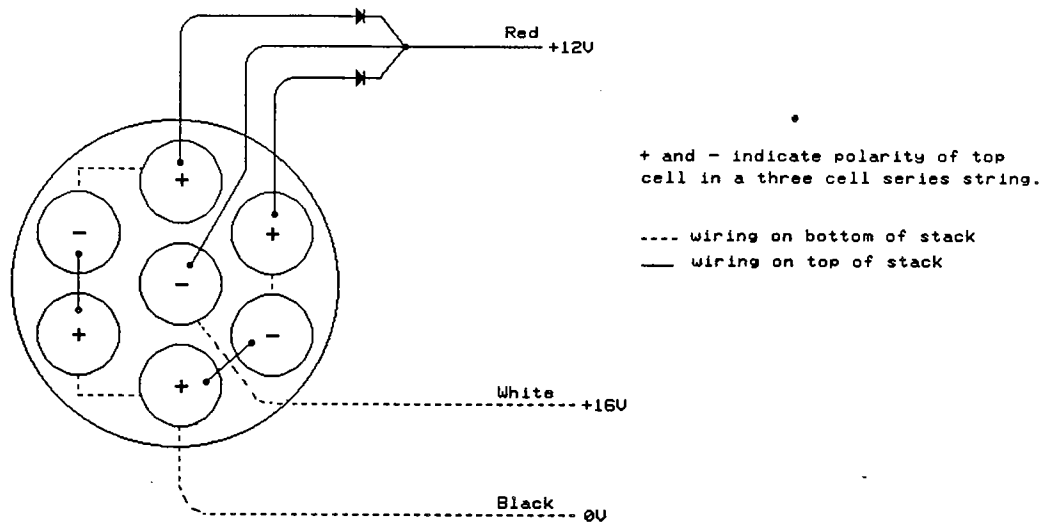
5.2 Back-Plane

Clip the white wire from the pin 5 end of the 10K ohm resistor located on the CAPACITOR card connector between pins 5 and 7. Connect this wire to pin 10 of the LOGIC card connector.

5.3 Battery Stack

Locate the 12 pin female MOLEX connector which exits the battery housing. Remove the orange wire from pin 1 of this connector, and discard it. Remove the red wire from pin 2 and place it in pin 1. Remove the white/red trace wire from pin 7 and place it in pin 2.

Refer to Figure 7. This is a schematic of the modified stack. Using twenty-one B1300-T2 alkaline cells and two 1N4002 diodes, construct such a stack and connect it to the molex connector as illustrated.



12 pin Female Molex
(Pin View)

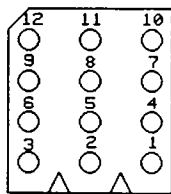
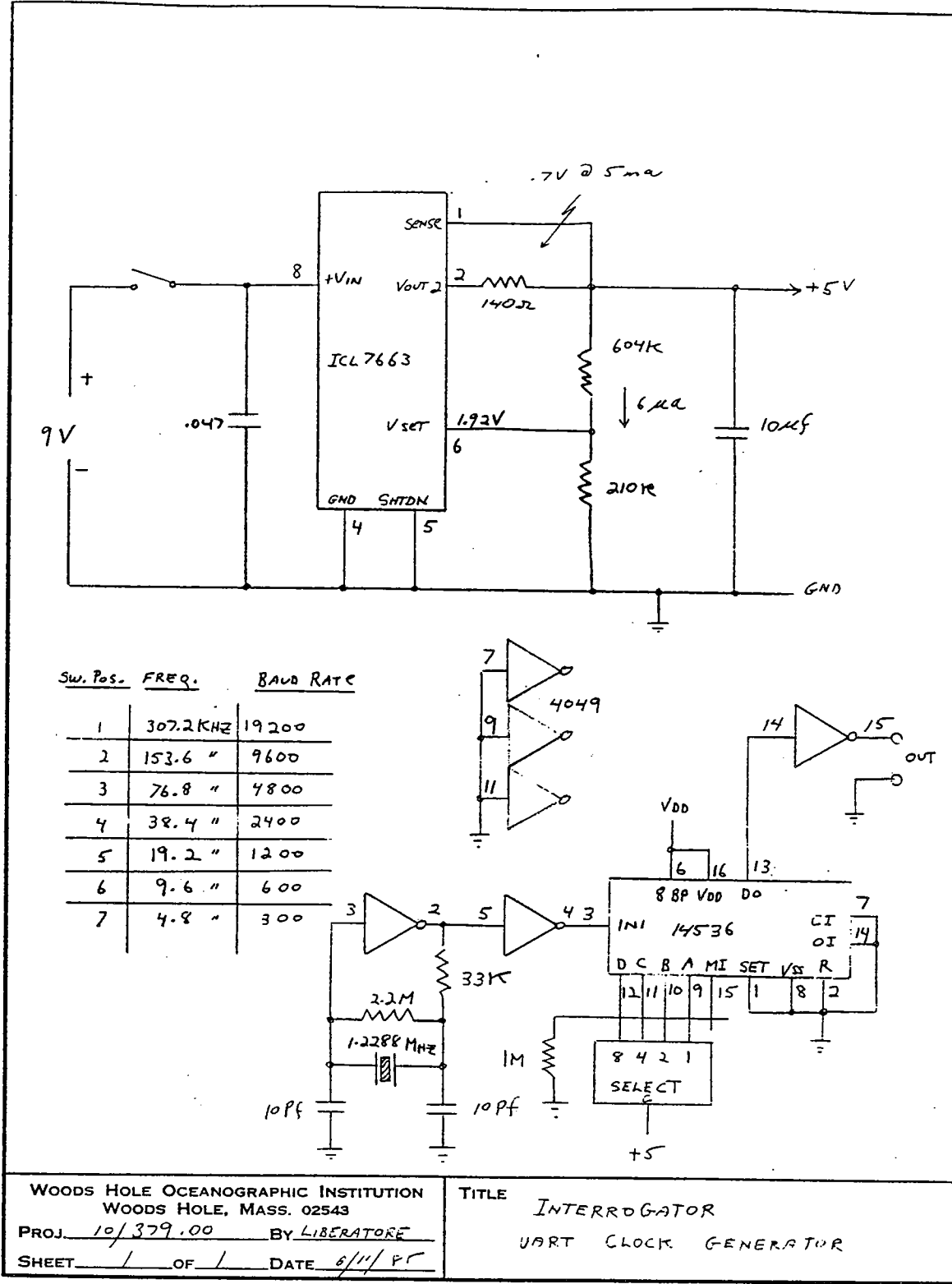


Figure 7: Interrogator Battery Pack



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TITLE INTERROGATOR
 UART CLOCK GENERATOR

SP 11200A

Figure 8 Interrogator UART Clock Generator

6.0 ACKNOWLEDGEMENTS

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